# Implementation of Non-Linear Controller for Contemporary DC-DC Converter

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*Abstract:* This article presents a analysis, design and implementation of non-linear controllers for fundamental negative super lift Luo-Converter (FNSLLC) for purposes needing the stable power source in battery operated portable devices, floppy/hard disk drives, LED TV, physiotherapy medical instrument, lap-top computers, mother board and fan in central processing unit (CPU) applications etc.,. The FNSLLC is a advanced DC-DC converter topology. The FNSLLC is erratic structure system (ESS) and its dynamic analysis is poor. The linear regulators for FNSLLC are poor operating analysis particularly during large source voltage and load modifications. With the aim of improve the dynamic analysis, load voltage and coil current controls of FNSLLC, a linear quadratic regulator (LQR) plus fuzzy logic controller (FLC) is designed. The LQR is designed for FNSLLC with their state space dynamic equations. The controller formation of this converter consists of two loops like, current loop (CL) and voltage loop (VL). In this study, LQR is act as a inner CL for manipulating the coil current of FNSLLC, but the FLC is act as a VL for controlling the load voltage of FNSLLC. The FLC is developed depending on the same system activities and qualitative linguistic control rules. The performance of FNSLLC using LQR plus FLC is verified at various operating states by building both in MATLAB/Simulink and prototype field programmable array (FPGA) models in comparisons with LQR plus proportional double integral controller (PDIC). The results and time domain specifications analyze are presented to prove the adroit of designed controller in different provinces.

*Keywords:* Super lift Luo-converter, Linear quadratic regulator, Fuzzy logic regulator, State Space Averaging Modeling.

## 1. Introduction

In current scenario, the development of automotive application and the digital world, there is an increase order of proficient DC choppers are utilized in many electronic systems such as portable electronic devices and other battery operated appliances, high gain, excellent quality, miniature in size, weightless, little prize, unswerving and capable power sources, which are indicates that the enormous research scope to DC choppers domain. The DC choppers are converting DC input voltage at one level to another level. Also, some its main constraints such as stumpy a.c waves in the voltage and current, good performance and simple structural design are provided so as to attain the precise output voltage regulation beside various constraint based on many applications such as low power source applications [1-2].
In conjectural tip of clarifications, basic DC choppers has obtain the high voltage gain with more duty cycle but in real time high duty cycle operation of choppers has produce serious reverse-recovery and EMI problems [2-3]. Based on above discussion problems, a voltage lift method have been effectively working based on design of DC choppers, in case, 3-sequence of Luo-Converters (LC), be subject to load voltage increases in summation progress. As a result, the super-lift system dramatically raises the voltage gain, in balanced evolution, then the prize of model difficulty, also compare to boost converter output voltage and current ripple should be reduced, where the fundamental negative super-lift Luo-converter (FNSLLC) can do the

same with configuration it has gorgeous DC-DC converter topology, that have been convert +ve source DC voltage to -ve output DC voltage in addition with feature of high efficiency, high power density, high gain and reduced coil current, output ripples compare to various predictable DC choppers [4]. In most of the conventional control methods namely linear controllers and fuzzy logic controller (FLC) etc. LC using PI controller providing decent characteristics. A PID control has non-capable ability in operating with system insecurity in the presence of overshoot and error in steady state problems and also, operation of PID-D is design with combination of PID and D controller. In order to overcome these problems new control technique will make to implement the propositional double Integral controller (PDIC) in this article. A FLC for the FNSLLC has been combined with PDIC to reduce the prattling phenomena. In the past most of the researches focus on sliding mode control (SMC) of the converter, in that control method the variables are chosen based on order of the FNSLLC that variables like current and voltage are preferred as closed loop purpose so there is an query on that the higher order converters are difficult to control by using low order controllers [5-9]. A novel control method consist of PDIC plus linear quadratic regulator (LQR) is used for output voltage and inductor current regulation of FNSLLC that are designed as inner and outer loop controllers, the inner loop regulate the inductor current and outer loop controller regulate output voltage in the circuit. In addition to that fine tuning of controller has to change the outer loop controller as FLC so as to minimize the steady state and dynamic response of FNSLLC to get the desired output parameters with all the disturbance formats. The designing of two loop controller an open operating system by adding hysteresis comparator in the same loop. This method was implemented by using index of performance of optimization based cost function. Most of the researchers have commenced to successfully utilize this method in the power electronics sectors [10]. The improvement of the projected loop-shaping controller not only focuses the benefits of the control strategy, to adjust the output response by the help of additional tuning parameters. The PDIC is commonly used in industrial sectors. Most of the researches are concentrate on output voltage regulation but in this article it will be achieved by designing robust controls for manipulating load voltage and coil current [11]. In common, the FNSLLC has complex system with circuit parameters variation that needs further valuable and proficient control methods for upcoming utility of application FNSLLC. Many surveys modeling approaches where testified for DC choppers. Amid which state space model was underlined as good mathematical method for DC choppers. The PI and PID for DC chopper where conversed [12]. The SMC in addition proportional double integral controller (PDIC) for FNOSLLC has been presented [13]. However, this method have produced more output voltage peak overshoots and long settling time during dynamic working conditions, more start-up overshoots, more design calculations, analog platform (SMC) and more number of sensors and non-satisfied overshoots were marked that is moderately unwanted, sensors also need large in number at the time of insistent for more calculations these type of problems are easily reduced by designing the alternate method linear quadratic regulator (LQR) based controller gain in feedback system discuss as follows [14-15], so in order to avoid these kind of problems by implementing the LQR controller based on performance indices are preferred with pole placement approach which mainly based on a perfect placement poles in the closed loop so this method had this drawback so in order to overcome this choose LQR controller which needs huge calculations and the cost function are arrived from the basic regulator are insight with non-uniform frequency and produced fastest dynamic performances [16]. To strengthen the LQR controller in addition to include the FLC in order to improve the dynamic characteristics of FNSLLC by using TS fuzzy models, the models are throughout the membership functions are designed to manipulate the parameters of the system and it has been shown in the literature survey [17].

The control design of frequency domain is the occurrence of RHPZ of plane shows that the range of coil (circuit) will be modify the position of null to little frequency side in direction of right of plane to create phase lag imprisons constant band width operation of converter possible resolution is providing of LQR controller which have systematic producer for addition of

control constraints foremost to strong regulation. The performance of the converter using PDI plus LQR controllers is estimated using MATLAB/Simulink as well as experimental. The results are presented and analyzed by applying digital control scheme to achieve current in continuous conduction mode (CCM) and calculation of duty cycle control in different ranges, several cases digital OCC approaches have been done but in this there is an imitating the integration part ,accumulator is used, calculate few samples of input current to get the average input current value for that we need fast and high resolution A/D converter, control every value of duty cycle has been reported [18].

From the above problems are solved by designed LQR plus FLC for FNSLLC. Therefore, in this article presents the design and experimental verification of LQR plus FLC for FNSLLC worked in CCM.

## 2. Design of FNSLLC

A new series of FNSLLC as shown in figure 1(a) which has high voltage transfer gain, high efficiency, low ripple voltage and current, and then two operating mode of this converter is explained as two states; one is switch on state and another one is switch off state are shown as figures 1(b) and 1(c), The circuit consists of DC input voltage $V_{in}$ , power switch (MOSFET) S, inductor L, capacitors $C_1$ and $C_2$ , freewheeling diodes $D_1$ and $D_2$, load resistance R. In ideal case, the operation of the FNSLLC in CCM to analysis the working states.
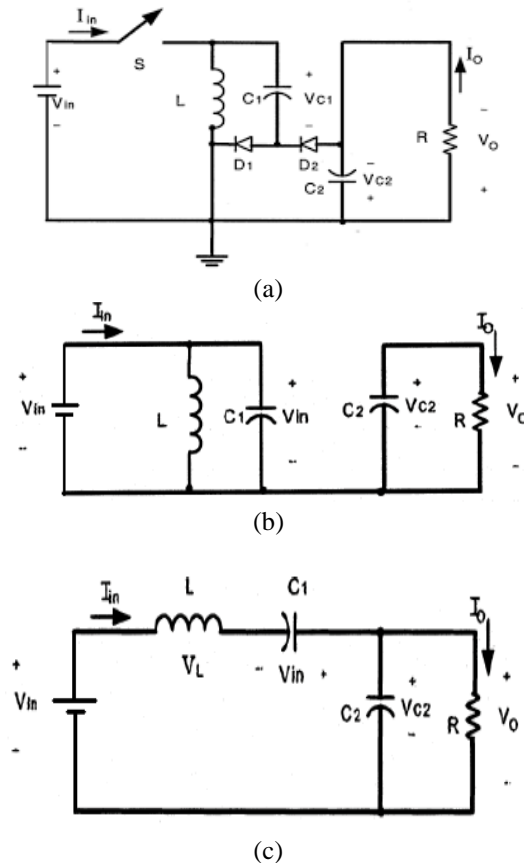


Figure 1(a). Topology of FNSLLC, (b). Mode 1 operation, (c). Mode 2 operation.

While the switch S is closed in mode 1, the $D_1$ forward polarized, the condenser is $C_1$ is energized upto $V_{in}$ at short time period and the capacitor voltage assume to be steady state value, then the slop of the inductor current increases with the ratio of $V_{in}$ /L and decreases with

slop – $(V_o\text{-}V_{in})/L$ during switch off (1-d) T the output capacitor $C_2$ delivers energy to the load resistance the equivalent circuit of FNSLLC state 1 shown in figure 1(b).

$$\begin{cases} L\,\dfrac{di_L}{dt}=V_{in} & \text{Switch ON} \\[2mm] C_2\,\dfrac{dV_o}{dt}=-\dfrac{V_o}{R} \end{cases} \tag{1}$$

During the state 2 operation, switch S is in open, $D_2$ conduct. Hence, the $i_L$ fall-offs amid the $C_1$ voltage $(V_o$– $V_{in})$ to deliver charge to $C_2$ and R. The FNSLLC in mode two 2 circuit is depict in figure 1 (c). The differential equations will be written as (2)

$$\begin{cases} L\dfrac{di_L}{dt}=2V_{in}-V_O & \text{Switch OFF} \\[2mm] C_2\dfrac{dV_O}{dt}=i_L-\dfrac{V_O}{R} \end{cases} \tag{2}$$

Applying charge capacitor balanced rule on $C_1$, the (3) for T as follow. Where, d is the control of the switch (d=1 when the S is closed, and d=0 when the S is open).

$$dC_1\frac{dV_{C1}}{dt}+(1-d)i_L=0 \tag{3}$$

In FNSLLC has a two capacitors which are $V_{c1}=V_{in}$, $V_o$, it is merely need to select by means of a state variable except $V_{in}$. Together by $i_L$, state variables of converter is nominated for $i_L$, and $V_o$ ($x_1$, and $x_2$). Applying above equations, the average modeling of the FNSLLC can extended as expressed by (4).

$$\begin{bmatrix} \dot{i}_L \\ \dot{V}_o \end{bmatrix}= \begin{bmatrix} 0 & -\dfrac{1-d}{L} \\[3mm] \dfrac{1-d}{C_2} & -\dfrac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_L \\ V_o \end{bmatrix}+ \begin{bmatrix} \dfrac{2-d}{L} \\[2mm] 0 \end{bmatrix}V_{in} \tag{4}$$

Where,
*A, B, C* and *D* are system state space matrices.

$$A=\begin{bmatrix} 0 & -\dfrac{1-d}{L_1} \\[3mm] \dfrac{1-d}{C_2} & -\dfrac{1}{RC_2} \end{bmatrix},\;\; B=\begin{bmatrix} \dfrac{2-d}{L} \\[2mm] 0 \end{bmatrix},\;\; C=[0\;\;1],\,D=[0\;\;0] \tag{5}$$

### A. Design calculation of FNSLLC parameters

The design starts with mathematical calculations that should be explained in detail from the FNSLLC parameters cataloged in Table 1. The design process has been represented in the form of flow chart figure 2, which will shows the calculations of various design parameters and specification of the circuits.

The FNSLLC constraints and phase-variable transformation are applied in (5). Later, *A, B, C,* and *D* matrices becomes

$$A=\begin{bmatrix} 0 & -\dfrac{1-d}{L_1} \\[3mm] \dfrac{1-d}{C_2} & -\dfrac{1}{RC_2} \end{bmatrix},\;\; B=\begin{bmatrix} \dfrac{2-d}{L} \\[2mm] 0 \end{bmatrix},\;\; C=[0\;\;1],\,D=[0\;\;0] \tag{6}$$

Table 1. The designed specification of the FNSLLC.

| Parameters name | Symbol | Value |
|---|---|---|
| Voltage (Input) | $V_{in}$ | 12V |
| Voltage (Output) | $V_o$ | -36V |
| Coil | $L$ | 100μH |
| Capacitors | $C_1, C_2$ | 30 μF |
| Nominal switching frequency | $f_s$ | 100kHz |
| Load resistance | $R_o$ | 40Ω-70Ω |
| Power (Output) | $P_o$ | 25.922W |
| Power (Input) | $P_{in}$ | 28.238W |
| Current (Input) | $I_S$ | 2.353A |
| Efficiency | $\eta$ | 91.8% |
| Current (Output) | $I_o$ | -0.72A |
| Ripple coil current | $\Delta i_L$ | 0.51A |
| Capacitor Ripple voltage | $\Delta V_o$ | -0.121V |

The flowchart and algorithm shows the FNSLLC, detailed calculation of parameters, which are helps to designing the converter,

Step 1: Select the duty cycle by using the formula.
Step 2: Calculate the output current $I_0$ and output power $P_0$.
Step 3: After that calculate the overall efficiency of the converter.
Step 4: Then we find out the input current by using above steps.
Step 5: Finally to calculate the circuit parameters by using design formulas
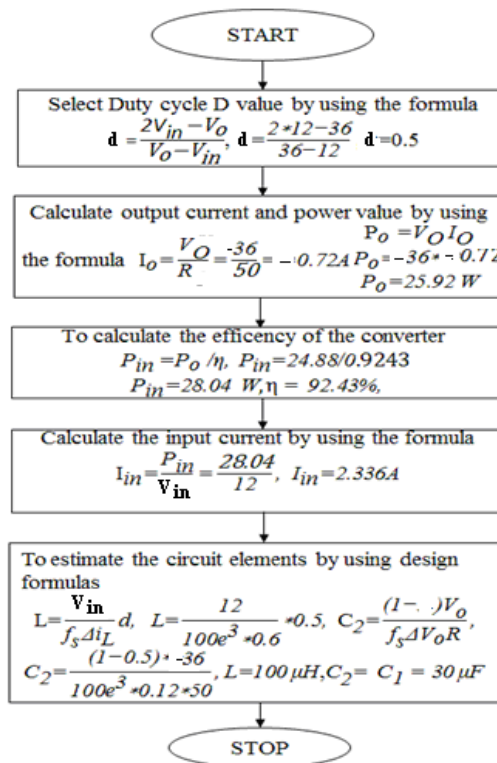


Figure 2. Flow chart for design calculation of FNSLLC

## 3. Development of feedback controllers for FNSLLC

The function of this segment is to discuss about the feed-back regulator for FNSLLC. The LQR cum PDIC/FLC technique for FNSLLC is exposed in **figure. 3**. This method having of two control loops namely, an inner current loop which has LQR for regulate $i_L$, and the outer voltage loop designed by using PDIC/Fuzzy to regulate $V_o$ of FNSLLC and to reduces steady state error. The $V_o$ and $i_L$ is measured from the output of the converter that measured signal is consider as error signal, the error signal indicates as $e_1$ and $e_2$, after that $e_1$ signal given input to PDIC/Fuzzy logic controller to regulate $V_o$ and reduces the steady state error. The error signal $e_2$ is given as input for the LQR controller to regulate $i_L$ and to generate reference current by considering output power and power loss. The signal indicate the control signal that is given to output of LQR that make the d of the switching pulse for driving the switch S of FNSLLC.
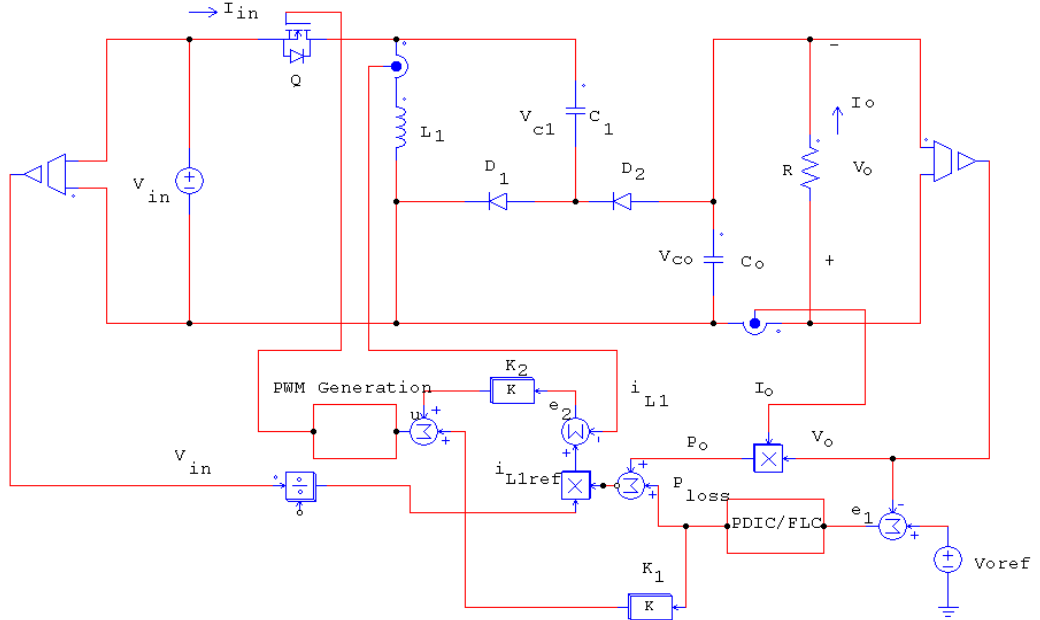


Figure 3. Control structure of the FNSLLC.

*A. Reference current generation*

The reference $i_L$ of FNSLLC is shown in the tree diagram as refer the figure 4. In tree diagram, it is clearly shows $P_{loss}$ specify the converter switching and resistive losses. Due to this loss in FNSLLC, the fall of capacitor $V_o$. While capacitor $V_o$ decreases along with the reference $V_o$, FNSLLC is not able to follow the reference inductor current closely. So, a suitable PDIC/FLC is inserted for this converter that controls the capacitor $V_o$ to the reference $V_o$ level, which is said as in the above figure 4. The $P_o$ is multiplication of $V_o$ and $I_o$ of FNSLLC.
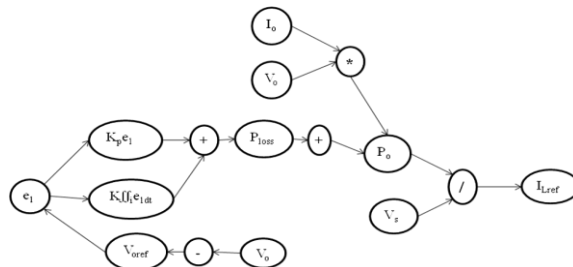


Figure 4. Tree diagram of generation of reference current.

*B. LQR (Detailed)*

The concept of maximize the control is complexity via. operating a running system at least cost. The time-in varying LQR is applied as tracking current regulator. In this study, LQR gain matrix for this converter estimated with proper preference values of R and Q (weight matrix). The Q and R matrices values are

$$Q = \begin{bmatrix} 2.161.1 \\ 1.11000 \end{bmatrix}, R = [1] \tag{7}$$

The Q matrix is selected in such a way that most weight age is applied to $i_L$, sequentially that $i_L$ of FNSLLC is controlled successfully via. LQR. The Q and R matrixes should be positive semi-definite and positive definite that are selected such that the scalar quantity xTQx is all the time positive or zero at every time t for the all functions x(t), and the scalar quantity uTRu is always positive at each time t for all values of u(t). In terms of eigen values, the eigen values of Q would be positive, whereas those of R could be positive. For a continuous time model the state-feedback control law u = −KF x minimizes the quadratic cost function;

$$J(x(.), u(.)) = \frac{1}{2} \int_{t_o}^{t_f} (x^T Q x + u^T R u) dt \tag{8}$$

Subject to the system dynamics

$$\dot{X} = AX + BU \tag{9}$$

For the developed converter, the quadratic cost function is found after substituting the values of X, Q, R in equation (8)

$$\int_{t_o}^{t_f} [(2.16x_1^2 + 2x_1 x_2 + 1000 x_2^2) + u^2] dt \tag{10}$$

The control law is found to be

$$u = -R^{-1} B^T K x = u = -K_F x \tag{11}$$

Where, KF is the feed-back controller gain matrix and K is the return function matrix. The unknown coefficients of the revisit function matrix are determined by solving the Ricatti equation.

$$K = A^* P + PA - PBR^{-1} B^* P + Q \tag{12}$$

On solving equation (12), the return function matrix K is found to be

$$K = \begin{bmatrix} K_{11} K_{12} \\ K_{21} K_{22} \end{bmatrix} = \begin{bmatrix} 2.21.1 \\ 1.11000 \end{bmatrix} \tag{13}$$

On substituting the value of K matrix in the equation, $K_F = -R^{-1}B^TK$ the feedback gain matrix $K_F$ is obtained. It is found to be [1.11 1000]

Therefore, the control law becomes

$$u = -1(x_{1ref} - x_1) - 1000(x_{2ref} - x_{ref}) \tag{14}$$

Once again the equation (14) becomes expressed as (15)

$$u = -(K_1 e_1 + K_2 e_2) \tag{15}$$

Where, $K_1$= 1.11 and $K_2$= 1000

*C. Design of FLC*

This part discuss about the FLC. At this point, the FLC (outer loop) that is applied to regulate power switch of FNSLLC. The inputs/output of this controller is described in figures. 5 (a) to (c). The voltage output error (e) and its change in error (ce) of FNSLLC is used as input of FLC and o (output) to generate the reference $i_L$ for it. For suitability, the numerical quantities of the inputs and output of FLC will be uniform and expressed as follows: e = [-1.11 -1.081 -1.061 -1.041 -1.021 0 1.021 1.041 1.061 1.081 1.11], ce = [-0.221 -0.141 -0.111 -0.0561 0 0.0561 0.111 0.141 0.221] and o = [-1.1 -0.0671 -0.04331 0 0.04331 0.0671 1.1] and its equivalent fuzzy sets are [NB, NM, NS, Z, PS, PM, PB] where, (negative big) NB, (negative small) NS, (zero) Z, (positive small) PS, (positive medium) PM, (positive big) PB, respectively. The membership functions of the e, ce, and o are illustrated in figure. 5. The rules of FLC selection are completely depending on FNSLLC characteristics. This article, forty nine rules are outlined and it recorded in Table 2. Then, the defuzzification process is applied to finish the fuzzy work with help of weighted average method.
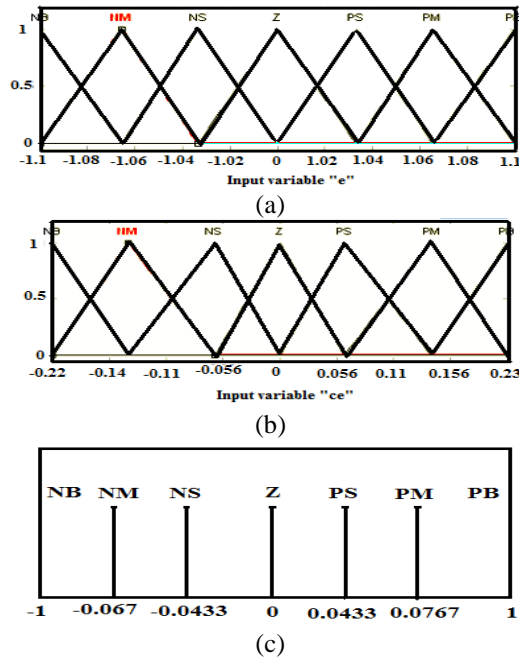
(a)



(b)



(c)

Figure 5. Membership's functions of FLC, (a) error (e), (b) change in error (ce),
and (c) output (o).

Table 2. Fuzzy rules of FNSLLC

| e / ce | NB | NM | NS | Z | PS | PM | PB |
|--------|----|----|----|----|----|----|----|
| NB | NB | NM | NB | NB | NM | Z | Z |
| NM | NB | NM | NB | NM | NS | NS | PM |
| NS | NB | NM | Z | Z | Z | PM | PS |
| Z | NB | NB | Z | Z | PS | PB | PM |
| PS | NM | NS | Z | PS | PS | PM | PB |
| PM | NS | Z | PS | PB | PM | PB | PB |
| PB | Z | PS | PS | PS | PB | PB | PM |

## 4. Results and discussions

The aim of this part is to deals about results of FNSLLC with LQR cum FLC in comparison with LQR cum PDIC at different operating condition with parameters are addressed in Table 1. The experimental block diagram model of the FNSLLC with LQR cum FLC/ PDIC is illustrated in figure.6. The details of the FNSLLC power circuits are as follows: S (IRFP 260 (MOSFET)); $D_1 - D_2$ FR306 (Diodes); $C_1 - C_2$ 30 μF/200V (polarized type) L 100μH/5A (Ferrite type).

The controller values are $K_1 = 1$, $K_2 = 0.089$, $K_p = 0.011$, $T_i = 0.0011s$ and 0.006121s as calculated using Ziegler Nicholas tuning method. The controller parameter of LQR cum FLC/PDIC is implemented in digital FGPA (dsPIC30F4011) controller platform (refer the figure. 6). In closed loop operation, measured values of $V_{in}$, $i_L$ and $V_o$ are scale down to smaller than ± 10V with help of signal conditioning circuit and isolation circuit. The analog to digital converter signals are routed by designed controller to compute d of power switch S. The PWM pulse is derived from dsPIC30F4011 and it is applied to trigger MOSFET of the FNSLLC using opto-coupler and driver IR2110. The main aim of the opto-coupler 6N137 is used for

isolation between the power circuit and control unit. The function of the driver circuit IR 2110 is utilized to magnify the pulses of the MOSFETs.
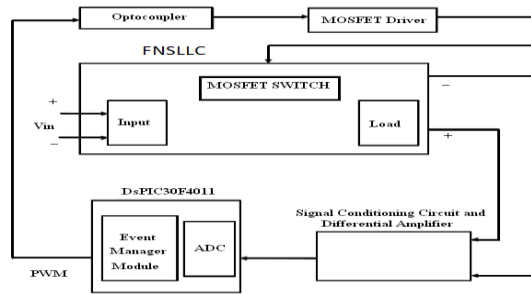


Figure 6. Experimental block diagram of FNSLLC with LQR cum FLC/PDIC.
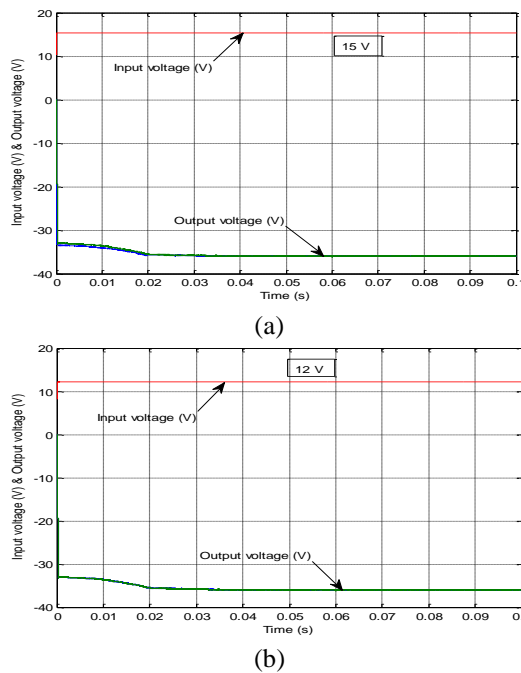
*A. Startup transient*



(a)



(b)

Figure 7. Simulated output and input voltage responses of FNSLLC in transient region using designed controllers (a).  LQR cum FLC and (b). LQR cum PDIC.

Figures 7 (a) and (b) show the simulated $V_o$ response of the FNSLLC for the nominal input voltages and load resistance via. LQR cum FLC (green color) and LQR cum PDIC (blue color) in start-up transient.  It is found that $V_o$ of FNSLLC via. LQR cum FLC has a null start-up overshoot and fast settling time, whereas the same model with LQR cum PDIC has generated null overshoots but settling time 0.015s in transient regions.

*B. Line variation*

Figure 8 (a) depicts simulated responses of $V_o$ and $V_{in}$ of FNSLLC via. LQR cum FLC and LQR cum PDIC for $V_{in}$ step change from 12V to 15V. From this figure, it is visibly showed that simulated $V_o$ response of FNSLLC via. LQR cum FLC was slight overshoot of -0.065V and minimal settling time, but the same system using LQR cum PDIC has created overshoots and long settling time.  Figure.8 (b) illustrates hardware responses of $V_o$ and $V_{in}$ of FNSLLC

via. LQR cum FLC for $V_{in}$ step change from 12 V to 15 V. It is noticeably identified that hardware results of $V_o$ of FNSLLC with LQR cum FLC has little peak of 0.09V and small settling time. Figure.9 (a) depicts simulated responses of $V_o$ and $V_{in}$ of FNSLLC via. LQR cum FLC for $V_{in}$ step change from 15V to 12V. It can be observed that response of $V_o$ of FNSLLC with LQR cum FLC have zero peak/settling time, while same system with LQR cum PDIC has produced overshoots and long settling time. Figure.9 (b) show the hardware responses of the $V_o$ and $V_{in}$ of FNSLLC with LQR cum FLC for $V_{in}$ step change from 15V to 12V (-20% line variations). It may be observed that experimental responses of $V_o$ of the FNSLLC via. LQR cum FLC have zero overshoot/settling time.
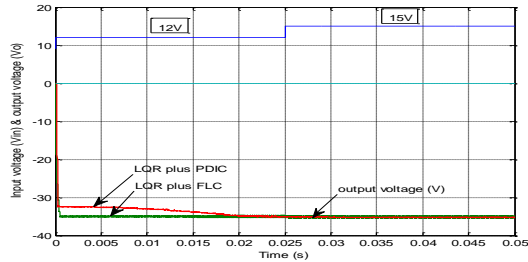


(a)
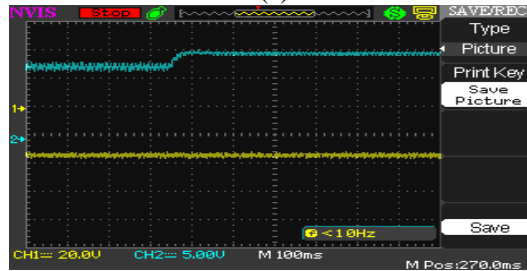


(b)

Figure 8. Output and input voltage responses of FNSLLC with controllers for $V_{in}$ change from 12V to 15V, (a). Simulation and (b). Hardware [CH1: - 20V/Div. $V_o$; CH2: 5V/Div. $V_{in}$].
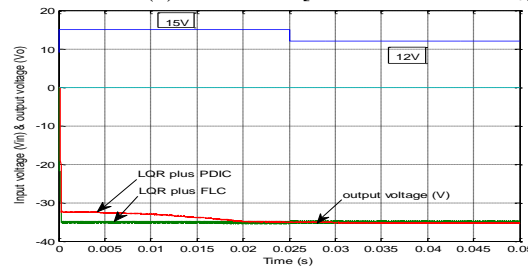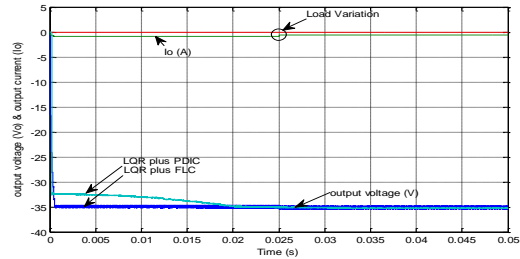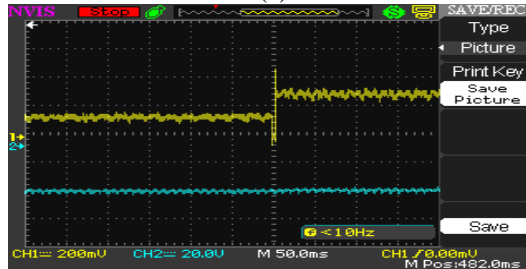


(a)
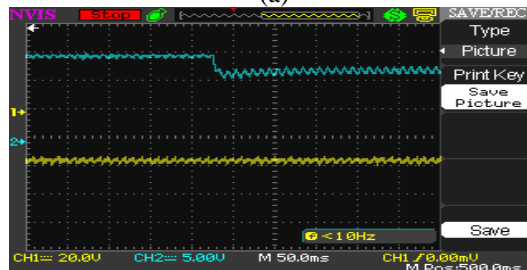


(b)

Figure 9. Output and input voltage responses of FNSLLC using designed controllers for input voltage step change from 15V to 12V, (a). Simulation and (b). Experimental [CH1: - 20V/Div. output voltage; CH2: 5V/Div. input voltage].
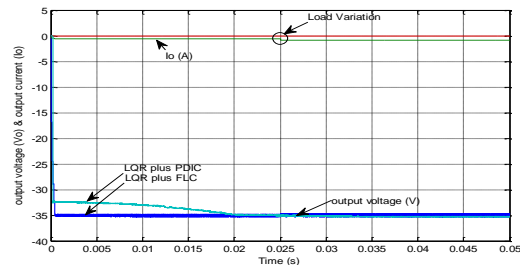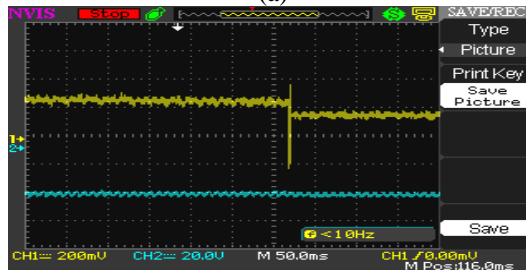
*C. Load variation*



(a)



(b)

Figure 10. Output voltage and current responses of FNSLLC using designed controllers for load resistance change from 40Ω to 60Ω, (a). Simulation and (b). Experimental [CH1: - 500mA/Div. output voltage; CH2: 20V/Div. input voltage].



(a)



(b)

Figure 11. Output voltage and current responses of FNSLLC using designed controllers for load resistance change from 60Ω to460Ω, (a). Simulation and (b). Experimental [CH1: - 500mA/Div. output voltage; CH2: 20V/Div. input voltage].

Figure 10. (a) show the simulated responses of $V_o$ and $I_o$ of FNSLLC via. controllers for R vary from 40Ω to 60 Ω (+20% load variations). It is found that simulation results of output voltage of the FNSLLC with this controller has a zero overshoot as well as fast settling time, while the same system using LQR plus PDIC has generated overshoots and long time to settle. Figure 10. (b) show experimental results of $V_o$ and $I_o$ of FNSLLC with LQR plus FLC for load

change 40Ω to 60 Ω (+20% load variations). It is found that the experimental results of $V_o$ and $I_o$ of FNSLLC using designed controller was zero overshoot as well as fast settling time.

Figure 11 (a) show the depict responses of $V_o$ and $I_o$ of the FNSLLC via. controllers for R vary from 60Ω to 40Ω (-20% load variations). It will be understood that the results of $V_o$ of FNSLLC with this controller has a zero peak overshoot as well as fast settling time over the LQR cum PDIC. Figure. 11 (b) show the experimental results of $V_o$ and $I_o$ of FNSLLC with LQR cum FLC for load change from 60Ω to 40 Ω. It can be understood that the experimental results of output voltage of the FNSLLC with designed controller has a zero overshoot as well as fast settling time.
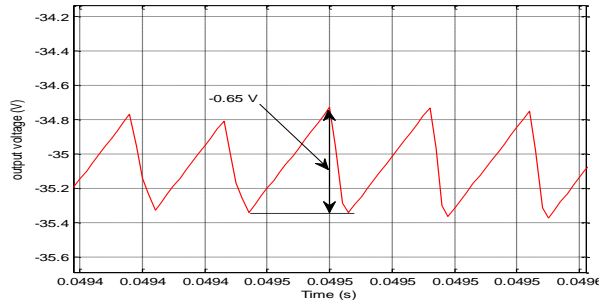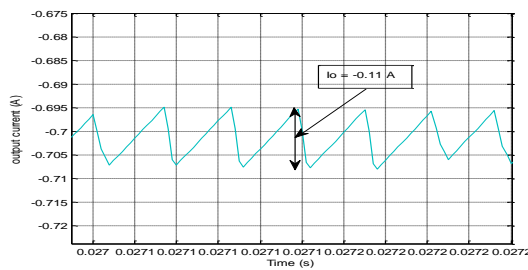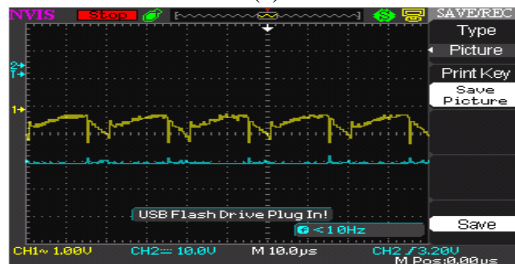
*D. Steady state region*



Figure 12. Simulated output voltage response of FNSLLC using designed controller in steady state region.

Figure 12 shows the simulation response instant output capacitor ripple voltage of the FNOSLLC in the steady state region using a LQR plus FLC. It is proof from the figure that the $V_o$ ripple is about -0.65 V for $f_s$ of 100 kHz. Figure. 13 (a) shows the simulated $I_o$ of FNSLLC in the constant mode region by a LQR cum FLC has produced ripple current of $I_o$ = -0.11A, which is closer to theoretical designed value (refer Table 1). Figure. 13 (b) shows the experimental result of output current and voltage ripples ($I_o$ =-0.13A & $V_o$ =-0.7V), which are match to theoretical designed values.



(a)



(b)

Figure 13. Simulated output current and voltage response of FNSLLC using designed controller in steady state region. (a) Simulation and (b). Experimental.
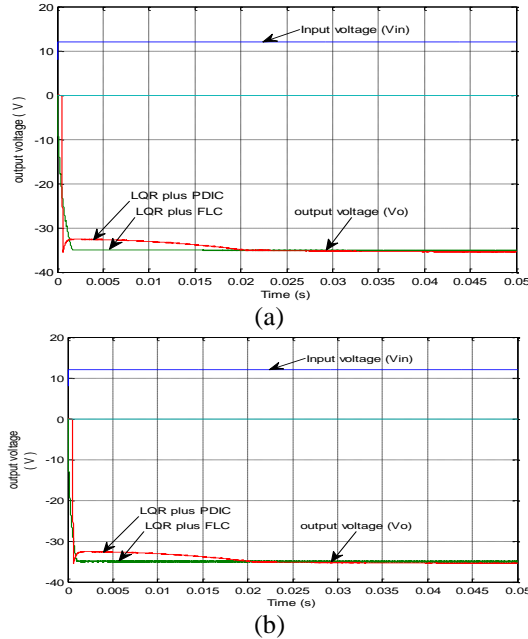
*E. Circuit components variations*



(a)



(b)

Figure 14. Simulated output voltage responses of FNSLLC using controllers in circuit components variations, (a) for inductor L variation from 100µH to 600µH and (b) for the change in capacitors ($C_1$ & $C_2$) ranges from 30µF to 100µF.

Figure 14 (a) represents the simulated responses of $V_o$ and $I_o$ of FNSLLC with a LQR cum FLC and LQR cum PDIC for inductor L variation from 100µH to 600µH. It could be found that change does not impact the FNSLLC performances due to a skilled designed controller. A fascinating result is shown in Figure. 14(b). It indicates $V_o$ and $I_o$ of FNSLLC responses using designed controllers for the change in capacitors ranges from 30µF to 100µF. It is found that the designed LQR cum FLC and LQR cum PDIC are effective in removing the cause of $C_1$ & $C_2$ modification except that a small peak and fast settling time.
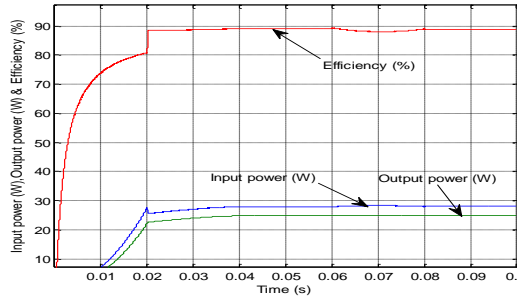
*F. Performance characteristics of the model*

Figures 15 (a), (b), and (c) shows the simulated and experimental performance characteristics of the FNOSLLC using a designed controller. It is visible that all the converter performance parameters were meet the theoretical specifications. Finally, the responses of FNSLLC with controller (designed) were carried out well at all operating states. Figure. 16. Experimental prototype model for FNSLLC using proposed controller.



(a)
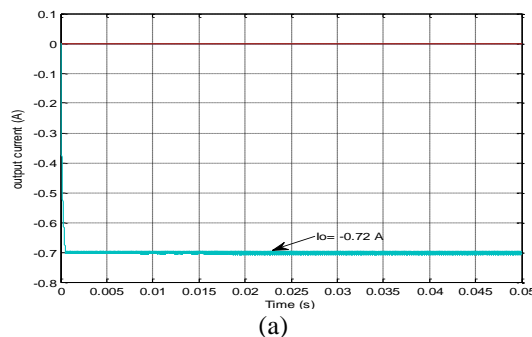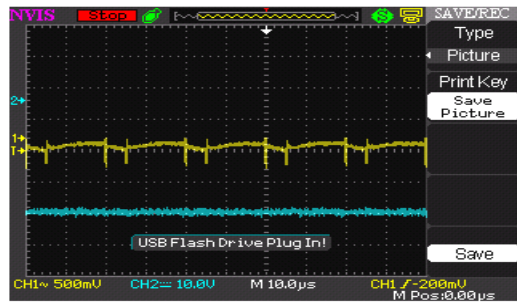
(b)



(c)

Figure 15. Output current, voltage, performance characteristics, and experimental model of FNSLLC using designed controller, (a). Simulation, (b). Experimental and (c). Output /Input powers, and efficiency.
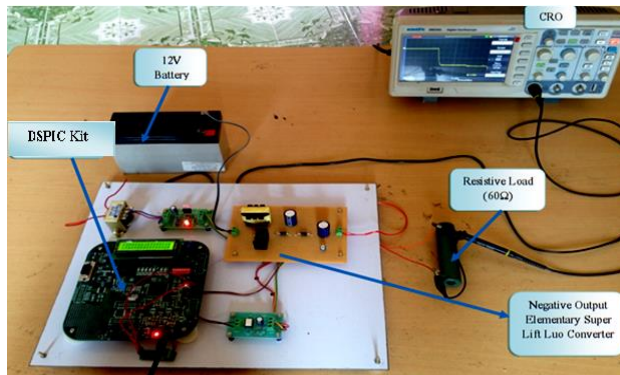


Figure 16. Laboratory prototype model for NOESLLC using LQR plus FLC in digital platform.

## 5. Conclusions

Thus, a design and implementation of LQR plus FLC for FNSLLC worked in CCM was effectively realized in Simulink as well as laboratory prototype models. The controller gains have been realized in digital (dsPIC30F4011) platform. The simulation and experimental responses were obtainable to exhibit victory of LQR cum FLC for FNSLLC outcome in excellent operating response, load regulation, and converter voltage is not affected in the circuit elements modifications, good steady state and magnificent start-up responses. Also, the designed controllers have produced excellent time domain specifications for this converter. Therefore, it is suitable for solar system, D.C micro grid, medical instruments and low/high power source applications.

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