Adaptive LMS Theory Based Energy Minimized Dynamic Voltage Restorer for Mitigating Various Power Quality Problems in a Distribution System

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Abstract: In this paper, Adaptive Least Mean Square (LMS) controller based Dynamic Voltage Restorer (DVR) is implemented to protect the sensitive loads from voltage related power quality issues (i.e. balanced voltage sag/swell, unbalanced voltage sag/swell and voltage harmonic distortion, etc.) in a three phase, three wire distribution system. Adaptive LMS theory is a well-known theory in the area of active shunt compensation. In this paper, this theory is adopted for the extraction of reactive and active power components of distorted source voltage which are the key components in the calculation of reference load voltage for the VSC of DVR. This control algorithm employs energy minimized voltage compensation which makes this DVR self-supported in nature i.e. there is no need for extra energy storage device and only capacitor is sufficient at DC bus of VSC. This phase locked loop (PLL) less control algorithm is very easy to implement, less complex and robust in nature. Few mathematical equations are required to implement this control algorithm in real time. The adopted control algorithm for DVR is verified in MATLAB by simulation studies and the real-time experimentation is done by using OPAL-RT under RT lab environment.

Index Terms: least mean square, dynamic voltage restorer, voltage sag/swell, total harmonic distortion, voltage quality problems and IGBT based VSC

1. Introduction

Modern industrial and domestic consumers assume clean and reliable power at their respective load centers. Many times, generating stations are not able to supply constant and clean power due to power quality issues [1]. Power quality is a wide term that contains many types of voltage as well as current related disturbances such as voltage sag, voltage swell, voltage unbalancing, voltage fluctuations, flickering, harmonics and poor power factor etc. at the point of common coupling (PCC) where the other sensitive loads are also connected [2-3]. For the compensation of the above-mentioned power quality issues, the role of custom power devices (CPD) is widely discussed in the literature [4]. There are three types of CPD_s such as a shunt connected CPD for the compensation of current quality problems known as distributed static synchronous compensator (D-STATCOM) [5], a series connected CPD for the compensation of voltage quality problems known as dynamic voltage restorer (DVR) [6] and combination of shunt and series CPDs for the compensation of current as well as voltage quality problems known as unified power quality conditioner (UPQC) [7]. Out of these CPD_s, DVR is used to shield the voltage sensitive loads such as medical equipments, semiconductor plants, paper mills, chemical plants, computer loads, microcontroller based loads and financial transaction systems, etc. from the voltage quality issues [3].

Basically, DVR is a series connected CPD which is connected between the grid station and critical load to provide the proper compensating voltage during grid voltage disturbances for maintaining the load voltage within the desired limit. Main components of DVR are an injection transformer, an energy storage device, an insulated gate bipolar transistor (IGBT) based voltage source converter (VSC), ripple filter and VSC side filter inductance. Basically, topology and rating of VSC of DVR depend upon the type of voltage compensation method used which includes pre-sag compensation [8,9], in-phase compensation [8,9] and energy minimized/quadrature compensation [8,9]. Each voltage compensation method has some advantages over others. As the name suggests, in energy minimized or the quadrature

Received: February 26th, 2020. Accepted: May 19th, 2021
DOI: 10.15676/ijeei.2021.13.2.8

compensation method, the DVR injected voltage is in quadrature with the line current so that the requirement of active power injection is negligible. This method can exchange the energy storage device by self-supported DC bus which will further decrease the cost of the overall system. But this method can't compensate the phase angle jump which makes it inefficient for the protection of phase sensitive loads.

Several topologies of the grid-connected DVR have been discussed in the literature [10-14] Nielsen et al. [10] proposed various topologies for DVR and a comprehensive comparison between different topologies is given. Komurcugil et al. [11] proposed an interesting transformerless topology for DVR which reduces the overall cost of the system. Al-hadidi et al. [12] proposed a new cascade-inverter based DVR, which has a capability to compensate a high and long duration voltage sag with little energy requirement from the cascaded inverter. For obtaining better transient as well as steady-state response, DVR_s based on superconducting magnetic energy storage [SMES] and an ultra-capacitor are presented in [13-14].

Various control algorithms for the better performance of DVR have been given in literature in detail [15-23]. Control algorithms for the capacitor-supported/self-supported DVR are given in [15-17]. Ghosh et al. [15] proposed a generalized control algorithm to maintain load voltage at its desired value even when the load is non-linear and unbalanced. Kanjiya et al. [16] and jayaprakash et al. [17] presented the control algorithm based on synchronous reference frame theory [SRFT] for the DVR to protect the voltage sensitive loads from grid voltage disturbances. SRF theory involves the source voltage transformation from rotating vectors to a stationary frame. A 3-phase phase-locked loop (PLL) is used for the synchronization purposes which makes this algorithm complex, hardly implemented in real time and difficult tuning of internal parameters such as proportional integral (PI) controllers. In [18], multilevel converter based DVR is discussed which employs predictive controller for better control purposes. Many other control algorithms such as fuzzy logic control [19], voltage elliptical compensation [20] and two degrees of freedom control [21] for controlling the DVR are discussed in detail. A modified EPLL based control of DVR is discussed in detail in [22]. An autonomous groups particle swarm optimization (AGPSO) based method is used to calculate the gains of DC link voltage PI controller as well as the load voltage PI controller. Pradhan et al. [23] proposed a dual PQ theory and instantaneous space phasor based control algorithm for the control of energy-optimized DVR.

On the other hand, adaptive least mean square (LMS) theory is a widely accepted theory for shunt current compensation [24-28]. Singh et al. [24-26] proposed a new Adaline (Adaptive Linear Element) algorithm for D-STATCOM. Adaline uses a least mean square (LMS) based algorithm to generate the reference source current for the VSC of D-STATCOM from the distorted and unbalanced load current. D-STATCOM is working satisfactorily for mitigation of various current related power quality problems to give load balancing, power factor correction, removal of harmonic current and neutral current compensation etc. Singh et al. [27] proposed the adaptive LMS based control algorithm for the grid-connected solar photovoltaic system. Singh et al. [28] proposed an adaline based LMS control algorithm to generate the fundamental frequency component of load current in three-phase shunt active power filter. This control algorithm is capable enough for compensation of reactive power, harmonic current and load unbalancing.

Adaptive LMS theory is not fully explored yet for the series voltage compensation. In this paper, this theory is adopted for the controlling of the DVR. The proposed algorithm is used to generate the reference load voltage for the VSC of DVR from the distorted and unbalanced source voltage. This control algorithm is capable enough to mitigate source side short as well as long duration voltage disturbances such as balanced sag/swell, unbalanced sag/swell and voltage harmonic distortion etc. There is no use of source voltage transformation and 3-phase PLL which make this algorithm very simple, robust, easily implementable in real time and having high convergence speed as well. The proposed control scheme for DVR is verified under MATLAB/SIMULINK software and real-time environment using OPAL-RT as well.

2. System Description and Design of DVR for Proposed Control algorithm

Figure 1(a) demonstrates the complete schematic diagram of grid-connected DVR which incorporates 3-phase programmable voltage source, VSC, filter, injection transformer and 3-phase critical load. To examine the consequences of line impedance, the supply voltage is measured at the point of common coupling (PCC). During voltage related power quality problems at the source side, the control algorithm provides the gate pulses for VSC to inject the correcting voltage through the injection transformer in order to achieve the constant and undistorted voltage at the load side. VSC energized by the DC link capacitance converts DC to PWM AC voltage and the filter is used to sweep out the switching harmonics from the inverter output. Figure 1(b) demonstrates the basic working principle of energy minimized voltage compensation for DVR at the time of sag in source voltage. The phasors V_s and V_s^* show the source voltage and sagged source voltages, respectively, whereas phasors V_L and V_L^* represent the load voltage before and after the sag. Phasors I_L and I_L^* are the load current before and after sag respectively. Load current (I_L) is taken as reference phasor to draw all the quantities. All the source voltage, load voltage and load current are phase-neutral quantities. θ is the phase lag of the source voltage during sag and β is the phase jump in load voltage during energy minimized compensation. The load current (I_L^*) phasor after sag is in perpendicular to the phasor of DVR injected voltage (V_{DVR}) in order to avoid the active power transfer between the DVR and grid. The source active power (P_{Source}) and desired load active power (P_{Load}) is defined as follows:

$$P_{Load} = 3V_L I_L \cos(\Phi) \tag{1}$$

$$P_{Source} = 3V_s^* I_L \cos(\Phi - \beta - \theta) \tag{2}$$

Where Φ is the load power factor angle.

In steady-state condition, the source will supply the total active power to the load by using the energy minimized voltage compensation method. However, during disturbances source will supply the maximum possible part of active power to the load in order to achieve minimum active power from the DVR which can be mathematically expressed as follows:

$$P_{DVR} = P_{Load} - P_{Source} = 0 \tag{3}$$

Substitute eq. (1) and (2) in (3)

$$\cos(\Phi - \beta - \theta) = \frac{V_L \cos(\Phi)}{V_s^*}$$

$$\beta = \Phi - \theta - \cos^{-1}\left(\frac{V_L \cos(\Phi)}{V_s^*}\right) \tag{4}$$

where $V_s^* \le V_L \cos(\Phi)$ must be satisfied,

Take $V_s^* = V_L \cos(\Phi)$,

Then, $\beta + \theta = \phi$ (5)

which means that the maximum sag that can be mitigated by the DVR is closely related to the load power factor [12]. The maximum amount of voltage sag which can be tackled by DVR is reported in the literature [10,12] and given as,

$$\Delta V_{sag} \le V_L\left(1 - \cos(\Phi)\right) \tag{6}$$

Basically, the design of DVR system parameters depends upon the grid parameters such as KVA rating of load, source voltage and frequency. The system components to be designed are: IGBT based VSC, DC link capacitance, rating and turns ratio of the transformer, ripple filter and AC side inductance [22,29,30].

A. Design and Selection of IGBT Based VSC

Voltage rating of IGBT based VSC of DVR depends upon the adopted voltage compensation method [8,9]. In this paper, energy minimized voltage compensation is used as clear from Figure 1(b). The magnitude of the DVR injected voltage can be calculated as:

$$V_{DVR} = \sqrt{(V_L^*)^2 + (V_s^*)^2 - 2V_L^* V_s^* \cos(\beta + \theta)} \quad (7)$$

All the voltages are phase-neutral quantities.

Substitute $\beta + \theta = \phi$ from eq. 5.

$$V_{DVR} = \sqrt{(V_L^*)^2 + (V_s^*)^2 - 2V_L^* V_s^* \cos(\phi)} \quad (8)$$

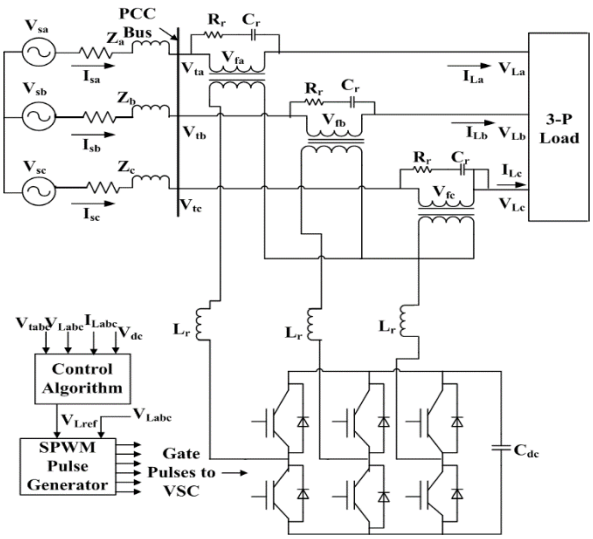
where, $V_L^* = 239V$, $V_s^* = 239 \times 0.8 = 191\text{V}$ (Source voltage during 20% sag), $\cos(\phi) = 0.8$ (Load lagging power factor)

$V_{DVR} = 143V$, the chosen value of $V_{DVR} = 150\text{V}$.

Current rating of VSC of DVR depends upon the 3-phase load rating. Considering the load of 10 KVA with 0.8 pf lagging, the current rating of VSC can be calculated as,

$3V_s I_s = 10000$, $V_s = 239\text{V}$ (Source voltage)

$I_s = 14A$



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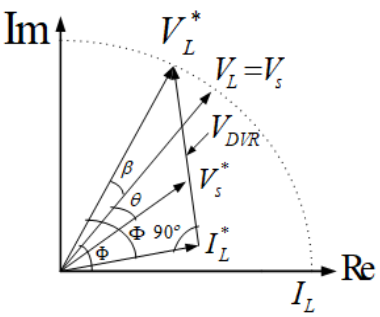


b.

Figure 1. (a) Schematic diagram of DVR (b) Phasor diagram of energy minimized voltage compensation for DVR

KVA rating of VSC of DVR can be calculated as reported in [22,30],

$$S = \frac{3 \times V_{DVR} \times I_s}{1000},\ V_{DVR} = 150V,\ I_s = 14A$$

$$S = 6.3\,\text{KVA}$$

B. Design and Selection of IGBT Based VSC

Selection of DC link capacitor is based on the transient energy required during the change in source dynamics [29,30]. During voltage related power quality problems at the source side, DC link capacitance absorbs or supplies the reactive power to maintain the load voltage at the desired value. Value of capacitance can be calculated as:

$$\frac{1}{2} c_{dc} \left[V_{dc}^2 - V_{dcf}^2 \right] = 3 \times V_{DVR} \times I_s \times \Delta t \quad (9)$$

where V_{dc} is the DC bus voltage, V_{dcf} is the change in DC bus voltage during the change in source dynamics and Δt is the required support time.

Take $V_{dc} = 300\text{V}$, $V_{dcf} = 300 - 3\%\ of\ 300V = 291\text{V}$, $I_s = 14A$, $V_{DVR} = 150\text{V}$ and $\Delta t = 0.002$. c_{dc} is calculated as,

$c_{dc} = 4271\mu F$, the chosen value of $c_{dc} = 4700\mu F$ (Standard Value)

C. Design and Selection of Injection Transformer

A three-phase injection transformer is used for this application in which VSC side windings are connected in star and line side windings are connected in series with each line. Design of injection transformer depends upon the compensated voltage required during voltage dynamics at source side [22,29,30]. Transformer is chosen such that the primary side (VSC) voltage is 70V and secondary side (Line-side) voltage is 150V. Selected rating of injection transformer can be calculated as:

$$\text{Injection Transformer } (KVA) = \frac{3 \times V_{DVR} \times I_s}{1000} \quad (10)$$

Where $V_{DVR} = 150\text{V}$ and $I_s = 14A$.

$KVA = 6.3\ KVA$, k=70V/150V

D. Design of Ripple Filter

A ripple filter is designed for removal of the harmonic frequency from the required compensated voltage of DVR. It comprises a series combination of a resister (R_r) and a capacitor (C_r). Tuning of this filter is done at half of switching frequency generally as:

$$f_r = \frac{1}{2\pi \times R_r \times c_r} \quad (11)$$

$f_r = f_s / 2 = 10000 / 2 = 5000Hz$,

Considering $R_r = 2\Omega$

$c_r = 16\mu F$

Hence, $R_r = 2\Omega$ and $c_r = 16\mu F$ are the appropriate values of ripple filter in this application

E. Design and Selection of AC Side Inductor

Rating of AC side inductance can be calculated as [30]:

$$L_r = \frac{k \times \sqrt{3}/2 \times V_{dc} \times m}{6 \times a \times f_s \times \Delta I_s} \tag{12}$$

where, transformer winding ratio k=70/150, VSC modulation index m=1, DC link voltage $V_{dc} = 300V$, ripple current in VSC $\Delta I_s = 14 \times 2\% I_s = 0.28$, switching frequency $f_s = 10\text{kHz}$ and overloading factor $a = 1.9$. L_r is calculated to be $4mH$.

3. Control Algorithm

In the area of active shunt compensation [24-28], Adaptive LMS theory is a broadly established theory. LMS and its variants are effectively used for controlling of D-STATCOM [24-26] and shunt active power filter [28]. In the active shunt compensation, adaptive LMS theory is used to generate the source current reference waveform from the distorted load currents effectively. In this paper, Adaptive LMS theory is adopted for the controlling of DVR and the equations involved in this theory are slightly modified. Reference load voltages ($V_{La}^*, V_{Lb}^*, V_{Lc}^*$) is generated from the active and reactive power components of distorted PCC voltages (V_{ta}, V_{tb}, V_{tc}). Schematic diagram of the control algorithm is shown in Figure 2. The basic equations involved in obtaining distinct control parameters of the control algorithm are shown as follows:

A. *Estimation of Amplitude Load Voltage and Load Current AS Well as Unit Templates*

Three phase load voltages are sensed to estimate the peak amplitude of load voltage as,

$$V_L = \sqrt{\frac{2}{3}(V_{La}^2 + V_{Lb}^2 + V_{Lc}^2)} \tag{13}$$

Three phase load currents are sensed to estimate the peak amplitude of load current as,

$$I_t = \sqrt{\frac{2}{3}(I_{La}^2 + I_{Lb}^2 + I_{Lc}^2)} \tag{14}$$

Unit templates in-phase to load current can be calculated as,

$$U_{pa} = \frac{I_{La}}{I_t}, U_{pb} = \frac{I_{Lb}}{I_t}, U_{pc} = \frac{I_{Lc}}{I_t} \tag{15}$$

Moreover, the load current in-phase unit current templates can be used to calculate the load current quadrature unit current templates as,

$$U_{qa} = \frac{U_{pc}}{\sqrt{3}} - \frac{U_{pb}}{\sqrt{3}}, U_{qb} = \left(\frac{U_{pb} - U_{pc}}{2\sqrt{3}}\right) + \frac{\sqrt{3}U_{pa}}{2}, U_{qc} = \left(\frac{U_{pb} - U_{pc}}{2\sqrt{3}}\right) - \frac{\sqrt{3}U_{pa}}{2} \tag{16}$$

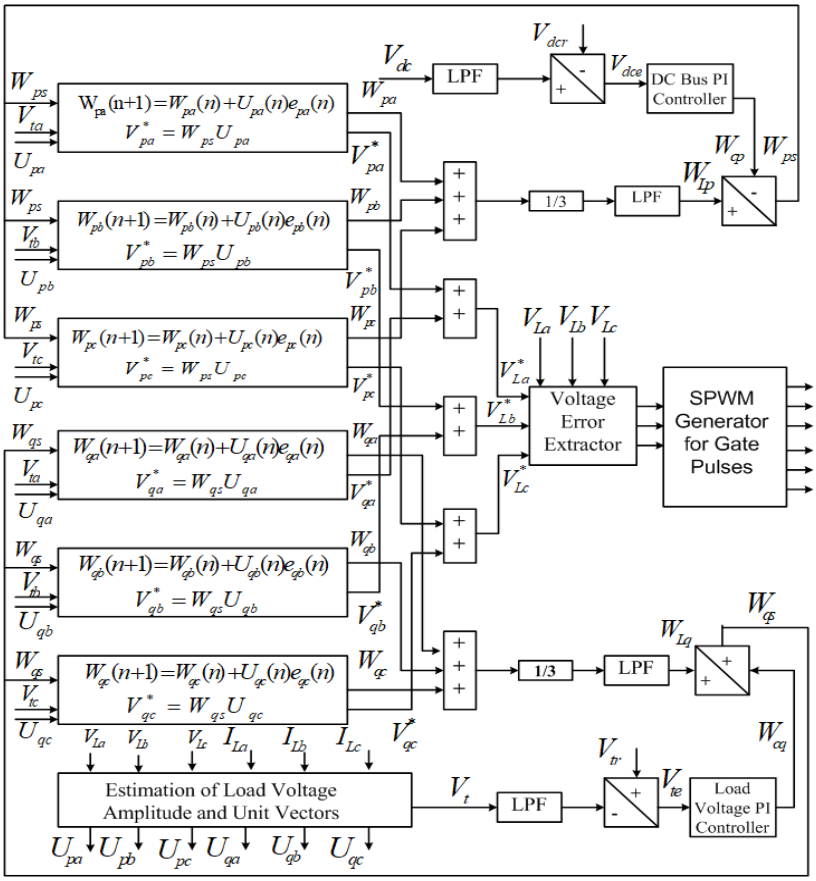


Figure 2. Adaptive LMS based control algorithm

B. Estimation of Weights of Fundamental Active and Reactive Power Components of PCC Voltage

The procedure for estimating weights of active components of PCC voltages, based on adaptive LMS algorithm, tracks the in-phase unit templates of load current to maintain minimum error ($e_{pa}(n)$). Weights of the fundamental active component of phase 'a' of PCC voltages at sampling time (n+1) th are calculated as:

$$W_{pa}(n+1) = W_{pa}(n) + U_{pa}(n)e_{pa}(n) \tag{17}$$

where $W_{pa}(n+1)$ corresponds to updated fundamental active weight component, $W_{pa}(n)$ corresponds to the previous weight, $e_{pa}(n)$ is an actual adaptive active component error of phase "a" is estimated as,

$$\mathrm{e_{pa}(n)} = \mu\left[V_{ta}(n) - U_{pa}(n)W_{pa}(n)\right] \tag{18}$$

where, μ (Adaptive constant/step size) is a very important parameter to decide the convergence rate of weight as well as the accuracy of estimation. The practical value of μ lies between 0.00001 to 1. A high value of μ leads to a high convergence rate of weight towards its optimum value but at the same time, it will result in an inaccurate estimate which will lead to high steady state error. A low value of μ increases the accuracy of estimation but decreases the convergence rate at the same time. The selected value of μ for this application equals to 0.002.

Similarly, the weights of the active component of phase "b" and phase "c" as well as their respective errors are expressed as,

$$W_{pb}(n+1) = W_{pb}(n) + U_{pb}(n)e_{pb}(n) \tag{19}$$

$$e_{pb}(n) = \mu\left[V_{tb}(n) - U_{pb}(n)W_{pb}(n)\right] \tag{20}$$

$$W_{pc}(n+1) = W_{pc}(n) + U_{pc}(n)e_{pc}(n) \tag{21}$$

$$e_{pc}(n) = \mu\left[V_{tc}(n) - U_{pc}(n)W_{pc}(n)\right] \tag{22}$$

The average value of weights of active components is obtained by adding eq. (17), (19) and (21) and passing it to low pass filter with cutoff frequency 10 Hz as,

$$W_{Lp} = \frac{W_{pa} + W_{pb} + W_{pc}}{3} \tag{23}$$

Weight of reactive component of phase "a" of PCC voltage at sampling time (n+1)th is calculated as,

$$W_{qa}(n+1) = W_{qa}(n) + U_{qa}(n)e_{qa}(n) \tag{24}$$

where $e_{qa}(n)$ is the actual adaptive active component error of phase "a" is calculated as,

$$e_{qa}(n) = \mu\left[V_{ta}(n) - U_{qa}(n)W_{qa}(n)\right] \tag{25}$$

where, μ is the adaptive constant/step size.

Similarly, the weights of reactive components of phase "b" and phase "c" of PCC voltage as well as their errors are expressed as,

$$W_{qb}(n+1) = W_{qb}(n) + U_{qb}(n)e_{qb}(n) \tag{26}$$

$$e_{qb}(n) = \mu\left[V_{tb}(n) - U_{qb}(n)W_{qb}(n)\right] \tag{27}$$

$$W_{qc}(n+1) = W_{qc}(n) + U_{qc}(n)e_{qc}(n) \tag{28}$$

$$e_{qc}(n) = \mu\left[V_{tc}(n) - U_{qc}(n)W_{qc}(n)\right] \tag{29}$$

The average value of weights of reactive components is obtained by adding eq. (24), (26) and (28) and passing it to low pass filter with cutoff frequency 10 Hz as,

$$W_{Lq} = \frac{W_{qa} + W_{qb} + W_{qc}}{3} \tag{30}$$

C. Calculation of Weights of Active as Well as Reactive Loss Components

The error between the peak amplitude of load voltage (V_L) and reference load voltage (V_{Lr}) is fed to a proportional-integral (PI) controller. Error at nth time instant is given as,

$$V_{Le}(n) = V_{Lr}(n) - V_L(n) \tag{31}$$

The output of this PI controller corresponds to the weight of the reactive loss component (W_{cq}), which is used to maintain the load voltage at its desired value.

$$W_{cq}(n+1) = W_{cq}(n) + K_{pL}\left[V_{Le}(n+1) - V_{Le}(n)\right] + K_{iL}V_{Le}(n+1) \tag{32}$$

where, K_{pL} and K_{iL} are the proportional and integral gains of load voltage PI controller.

Further, The error between DC link voltage (V_{dc}) and reference load voltage (V_{dcr}) is fed to a proportional-integral (PI) controller. Error at nth time instant is given as,

$$V_{dce}(n) = V_{dcr}(n) - V_{dc}(n) \tag{33}$$

The output of this PI controller corresponds to the weight of the active loss component (W_{cp}), which is used to maintain the DC link voltage at its desired value.

$$W_{cp}(n+1) = W_{cp}(n) + K_{pd}\left[V_{dce}(n+1) - V_{dce}(n)\right] + K_{id}V_{dce}(n+1) \tag{34}$$

where, K_{pd} and K_{id} are the proportional and integral gains of DC link voltage PI controller.

D. Generation of Reference Three-Phase Load Voltages

The total active weight component (W_{ps}) of reference three-phase load voltages can be calculated by subtracting active loss component from average fundamental active weight component as,

$$W_{ps} = W_{Lp} - W_{cp} \tag{35}$$

The active components of reference load voltage are obtained as,

$$V_{pa}^{*} = W_{ps}U_{pa},\ V_{pb}^{*} = W_{ps}U_{pb},\ V_{pc}^{*} = W_{ps}U_{pc} \tag{36}$$

Similarly, the total reactive weight component of reference three-phase load voltage can be calculated by adding the reactive loss component to the average fundamental reactive weight component as,

$$W_{qs} = W_{cq} + W_{Lq} \tag{37}$$

The reactive components of reference load voltage are obtained as,

$$V_{qa}^{*} = W_{qs}U_{qa},\ V_{qb}^{*} = W_{qs}U_{qb},\ V_{qc}^{*} = W_{qs}U_{qc} \tag{38}$$

Finally, the total three-phase reference load voltages are calculated as,

$$\begin{aligned} V_{La}^{*} &= V_{pa}^{*} + V_{qa}^{*} \\ V_{Lb}^{*} &= V_{pb}^{*} + V_{qb}^{*} \\ V_{Lc}^{*} &= V_{pb}^{*} + V_{qc}^{*} \end{aligned} \tag{39}$$

E. Generation of Gate Pulses Using SPWM Controller

The error voltage signal is generated from the difference between the reference load voltages ($V_{La}^{*}, V_{Lb}^{*}, V_{Lc}^{*}$) and sensed load voltages (V_{La}, V_{Lb}, V_{Lc}). These error signals processed by the sinusoidal pulse width modulator (SPWM) controller which is operated on 10 KHz frequency to generate the gate pulses for VSC of DVR.

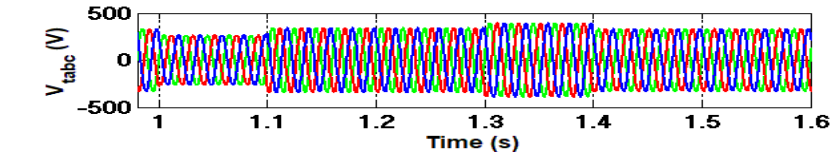
4. Simulation Results

Adaptive LMS control algorithm based DVR simulation model is developed in the MATLAB/Simulink environment. A critical 10 KVA, 0.8 pf load is adopted for the study. The performance investigation of adaptive LMS control algorithm based DVR has been carried out under various source-side voltage quality problems such as balanced voltage sag, balanced voltage swell, unbalanced voltage sag, unbalanced voltage swell, voltage harmonic distortion, balanced voltage sag with harmonic distortion, balanced voltage swell with harmonic distortion, unbalanced voltage sag with harmonic distortion and unbalanced voltage swell with harmonic distortion . System parameters taken for the simulation study are given in the Appendix.

A. Intermediate Signals of Adaptive LMS Control Algorithm and Generation of Reference Load Voltage for DVR

Various disturbances in the source voltage such as balanced voltage sag (i.e., 1.0s to 1.1s), voltage harmonic distortion (i.e., 1.2 s to 1.3 s) and balanced voltage swell (i.e., 1.3 s to 1.4 s) are added to show the response of intermediate signals of adaptive LMS control algorithm as shown in Figure 3 to Figure 6. At the time of source side disturbance, the function of the control algorithm is to provide the gate pulses for the VSC of DVR to produce the compensating voltage and protect the sensitive load form these disturbances. The error between the reference load voltage and actual load voltage is needed by the SPWM controller to generate the gate pulses for the VSC of DVR. Figure 3 to Figure 6 demonstrate the signals required to generate the reference load voltage. Subplots 1 to 4 of Figure 3 shows the PCC voltages (V_{tabc}), the average value of active components of source voltage (W_{Lp}), DC link voltage PI controller output (W_{cp}) and the

signal (W_{ps}) which is the result of subtraction of signals (W_{Lp}) and (W_{cp}) respectively. (W_{ps}) is multiplied by the unit in-phase templates of the load current of phase (a), (b) and (c) to generate the active component (V^*_{pabc}) of reference load voltage as shown in subplot 1 of Figure 4. Subplots 2 to 4 of Figure 4 shows the average value of reactive components of source voltage (W_{Lq}), AC voltage PI controller output (W_{cq}) and the signal (W_{qs}) which is the result of the addition of signals (W_{Lq}) and (W_{cq}) respectively. (W_{qs}) is multiplied by the unit quadrature templates of the load current of phase (a), (b) and (c) to generate the reactive component (V^*_{qabc}) of reference load voltage and active as well as reactive power required during compensation as shown in Subplots 1 to 3 of Figure 5. DVR active power settling time is only 0.05 s, which shows the excellent dynamic performance of the proposed control algorithm. Three-phase reference load voltage (V_{Lref}) is computed by adding (V^*_{pabc}) and (V^*_{qabc}) as shown in subplot 4 of Figure 5. Subplot 1 to 2 of Figure 6 shows the actual sensed load voltage (V_{Labc}) and the error ($V_{Le(abc)}$) between the reference load voltage and sensed load voltage. This error signal of three phases has to pass to the 3-phase SPWM controller to produce the six control pulses to the VSC of DVR so that DVR mitigates source side voltage related power quality problems.



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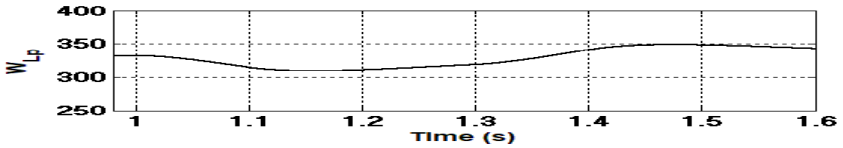

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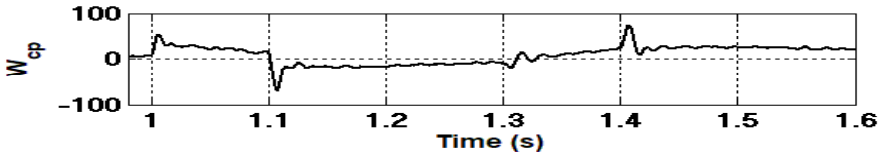

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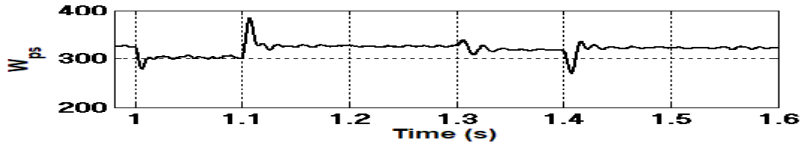


(d).

Figure 3. (a) PCC voltages (V_{tabc}) (b) Average value of active components of source voltage (W_{Lp}) (c) DC link voltage PI controller output (W_{cp}) (d) W_{ps}(Result of subtraction of signals (W_{Lp}) and (W_{cp}))

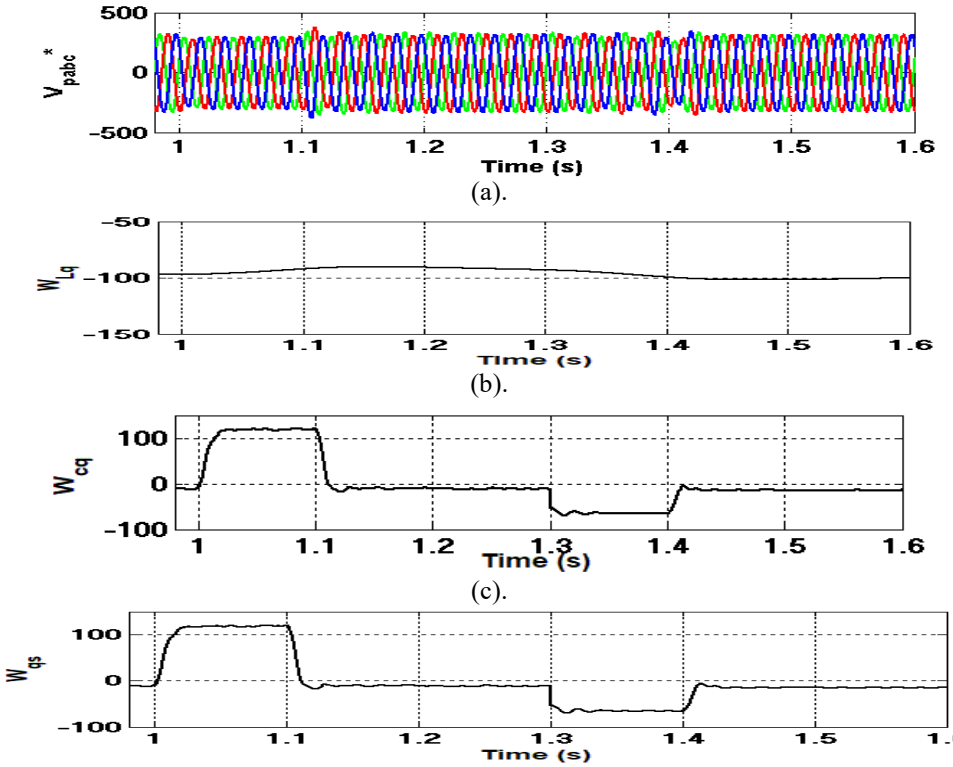
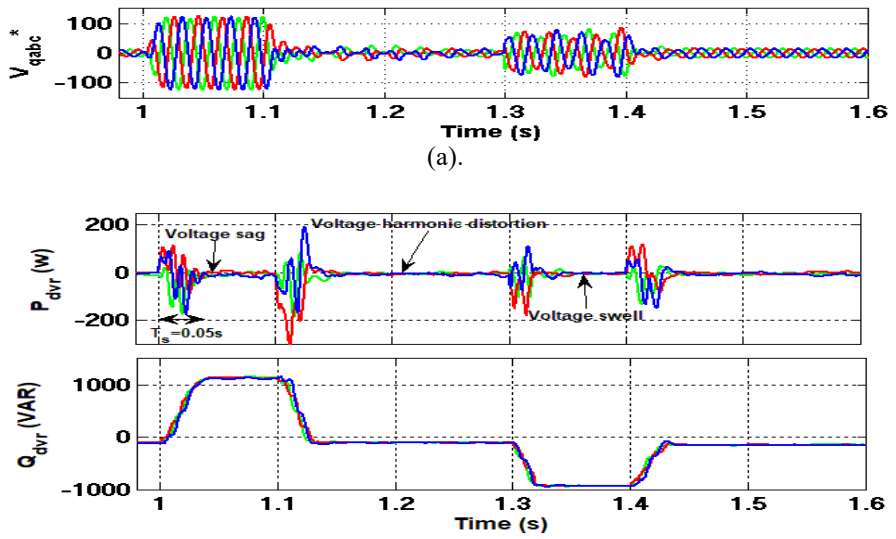
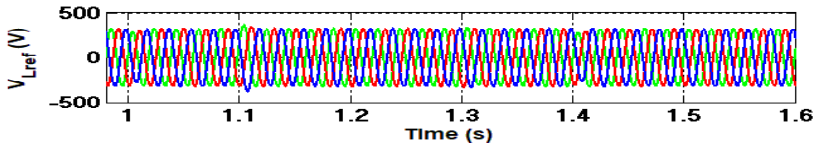


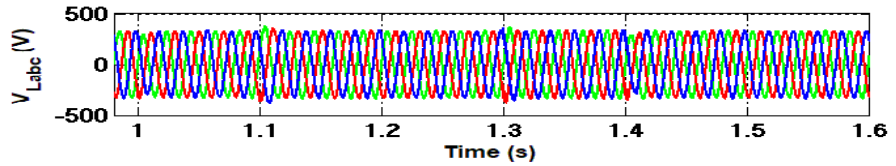
Figure 4. (a) Active component of reference load voltage ((V^*_{pabc})) (b) Average value of reactive components of source voltage (W_{Lq}) (c) AC voltage PI controller output (W_{cq}) (d) W_{qs} (Result of the addition of signals (W_{Lq}) and (W_{cq}))



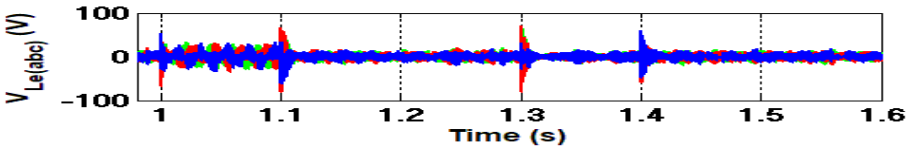


(c).

Figure 5. (a) Reactive component of reference load voltage (V^{*}_{qabc}) (b) Required active power during compensation (P_{dvr}) (c) Required reactive power during compensation (P_{dvr}) (d) Reference load voltage (V_{Lref})



(a).



(b).

Figure 6. (a) Actual load voltage (V_{Labc}) (b) error between the reference load voltage and sensed load voltage ($V_{Le(abc)}$)

B. Performance Investigation of DVR with Various Source Side Voltage disturbances

To check the validity of the proposed adaptive LMS control algorithm, the performance of DVR is tested under various source voltage disturbances. DVR performance during 20% balanced voltage sag (i.e., 1s to 1.05s), 20% unbalanced voltage sag in two phases (i.e., 1.1s to 1.15s), 20% balanced voltage sag with harmonics distortion (i.e., 1.2s to 1.25s), voltage harmonic distortion (i.e., 1.25s to 1.3s) and 20% unbalanced voltage sag in two phases with harmonics distortion (i.e., 1.3s to 1.35s) shown in Figure 7 to Figure 8. Subplots 1 to 4 of Figure 7 show the PCC terminal voltage (V_{tabc}), DVR injected voltage (V_{fabc}), undistorted load voltage (V_{Labc}) and undistorted source current (I_{sabc}) during the above-mentioned voltage disturbances. It is clear from the results that DVR injects the proper compensating voltage during source disturbances and protects the sensitive load from these disturbances. Subplots 1 to 3 of Figure 8 show the amplitude of PCC voltage as well as load voltage, the reference load voltage and DC link voltage during disturbances.

The performance of DVR is also tested for balanced/unbalanced voltage swell along with voltage harmonic distortion. Figure 9 shows that a balanced voltage swell of 20% magnitude occurs at 1 s and continue till 1.05 s, after that an unbalanced voltage swell in two phases of 20% magnitude occurs at 1.1 s and continue till 1.15 s. This is followed by a voltage harmonic distortion along with balanced/unbalanced swell occurs between 1.2 s to 1.35 s. Subplots 1 to 4 of Figure 9 show the PCC terminal voltage (V_{tabc}), DVR injected voltage (V_{fabc}), undistorted load voltage (V_{Labc}) and undistorted source current (I_{sabc}) during the above-mentioned voltage disturbances. Subplots 1 to 3 of Figure 10 show the amplitude of PCC voltage as well as load voltage, reference load voltage and DC link voltage during disturbances. Subplots 1 to 4 of Figure 11 show the PCC voltage, the harmonic spectrum of PCC voltage, load voltage and harmonic spectrum of load voltage as well. It is also observed from the results that the total harmonic distortion (THD) in load voltage is within the limit (i.e., THD < 5%) according to IEEE-519 standard under various source side voltage disturbances.

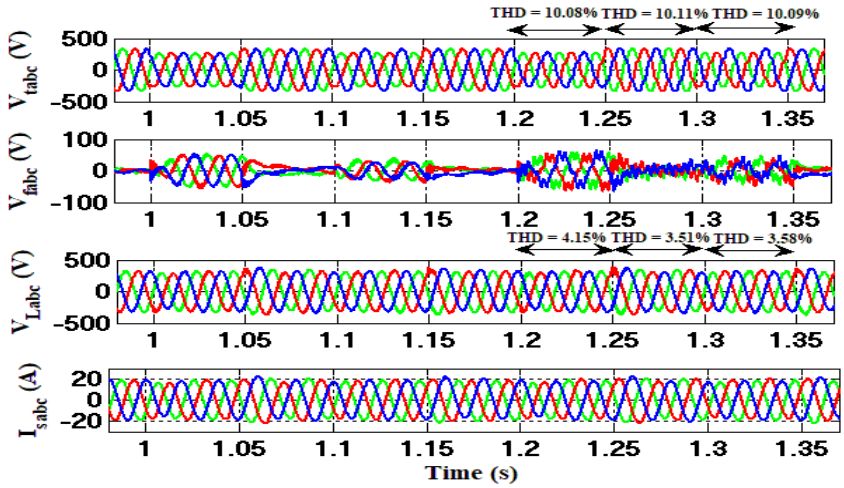


Figure 7. (a) PCC terminal voltage (V_{tabc}) (b) DVR injected voltage (V_{fabc}) (c) Load voltage (V_{Labc}) (d) Source current (I_{sabc})

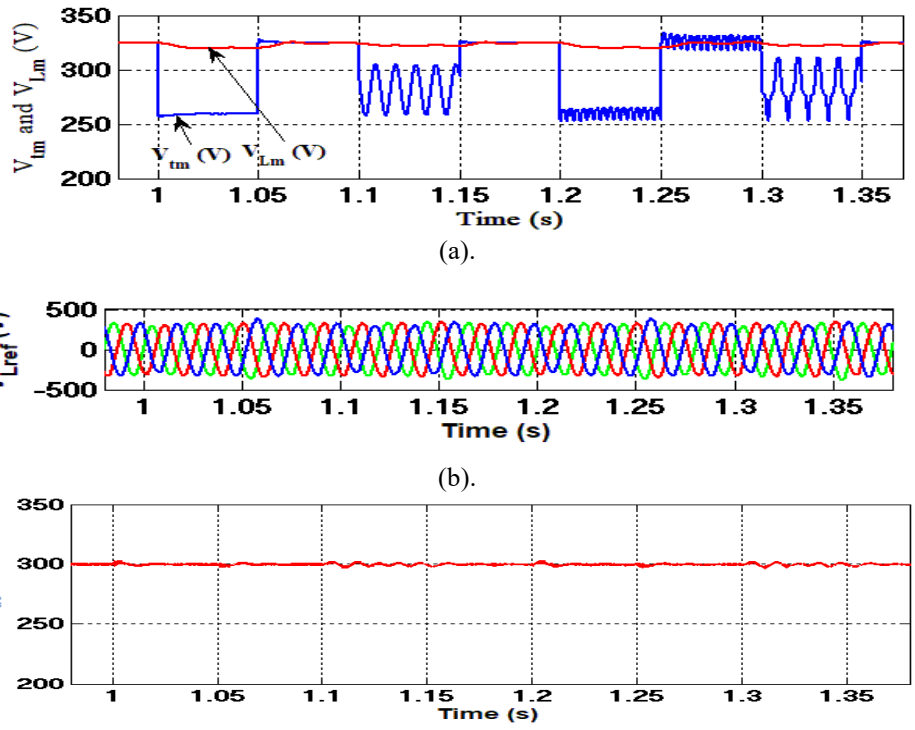


Figure 8. (a) Amplitude of PCC voltage as well as load voltage (b) Reference load voltage (V_{Lref}) (c) DC link voltage (V_{dc})

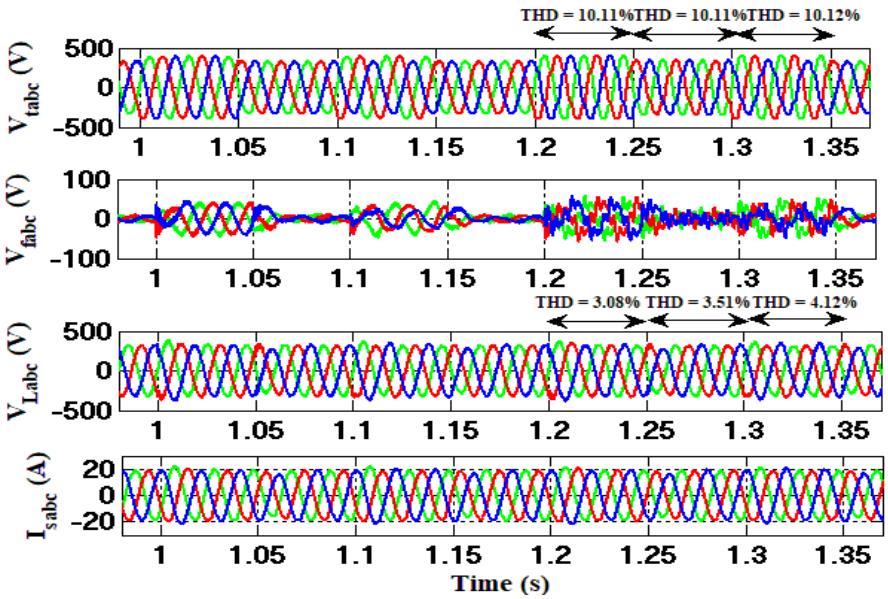
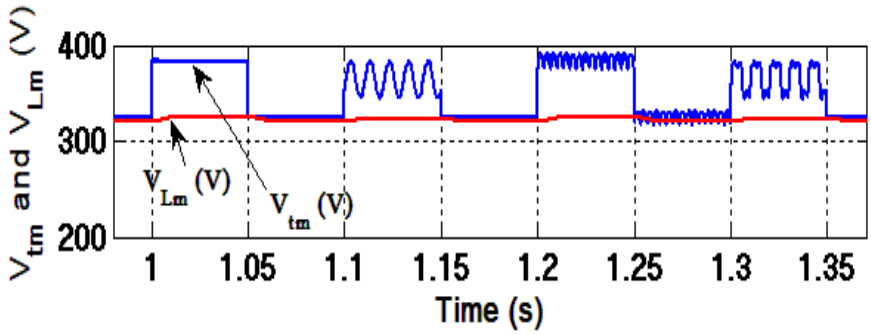


Figure 9. (a) PCC terminal voltage (V_{tabc}) (b) DVR injected voltage (V_{fabc}) (c) Load voltage (V_{Labc}) (d) Source current (I_{sabc})



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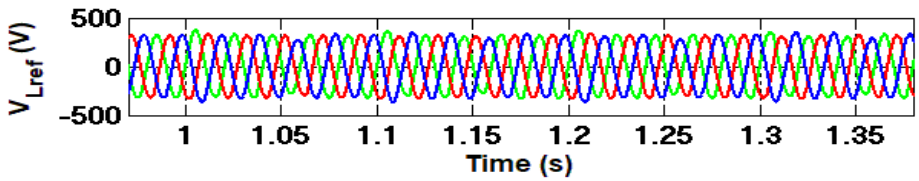

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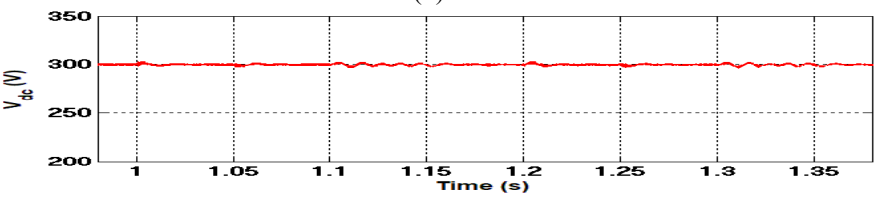
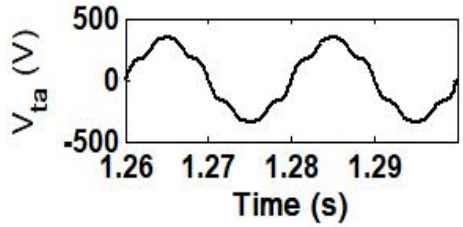


(c).

Figure 10. (a) Amplitude of PCC voltage as well as load voltage (b) Reference load voltage (V_{Lref}) (c) DC link voltage (V_{dc})



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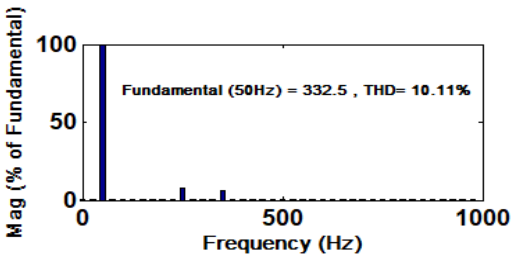

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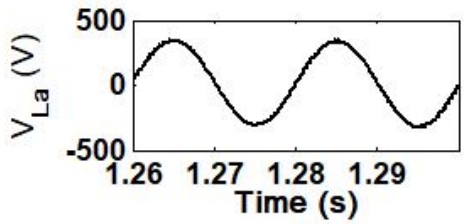

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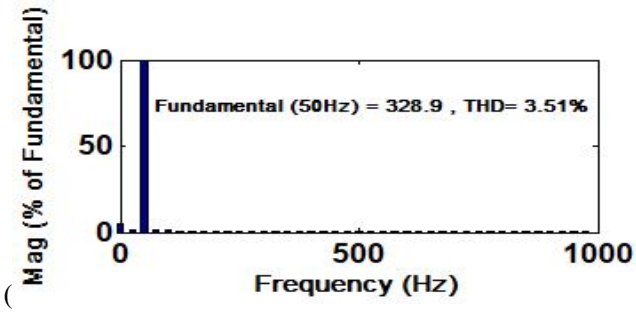


(d).

Figure 11. (a) PCC voltage during voltage harmonic distortion (b) THD spectrum of PCC voltage (c) Load voltage (d) THD spectrum

C. Comparative-Analysis of Proposed Adaptive LMS Based Control with SRFT Algorithm

A comparative analysis of adaptive LMS with SRFT control algorithm based on two criteria i.e. extraction of the fundamental active component of source voltage during source unbalancing condition and DC link voltage dynamics during transient as well in the steady state has been done. Figure 12(a) shows the dynamics of the average weight of fundamental active component of source voltage when subjected to an unbalanced sag in two phases for the conventional SRFT based control algorithm as well as proposed adaptive LMS based control algorithm. It is observed that oscillations in $W_{Lp}$are very less during the transient state as well as during source unbalancing when compared to oscillations in "W_{Lp}"signal with conventional SRFT based control. A detailed comparison between the two control algorithms in relation to the extraction of the fundamental active component of the source voltage is given in detail in Table-1. Figure

12(b) shows the dynamics of the DC link voltage. This figure clearly indicates that the proposed adaptive LMS algorithm is taking less time to stabilize the DC bus as compared to conventional SRFT based algorithm. A comparative analysis between the two above discussed control algorithms has been done in terms of rise time (T_r), settling time (T_s) and maximum overshoot (M_p) and details of the comparison are given in detail in Table-2.

Table 1. Comparative analysis between proposed (Adaptive LMS) and SRFT based algorithms in relation to the extraction of the fundamental component of the source voltage

Parameters	SRFT based control algorithm	Proposed adaptive LMS based control algorithm
Type	Time-domain, PLL based	Adaptive filter, PLL-less
Reference frame transformation	Yes	No
Number of computations	More	Less
Order of optimization	NA	Second
Computational burden	High	Low
Oscillations during transient	High	Very low
Oscillations during source unbalancing	Very high	Very low
THD of load voltage during balanced/unbalanced sag with harmonics in source voltage	5.60%, 4.48%	4.15%, 3.58%
THD of load voltage during balanced/unbalanced swell with harmonics in source voltage	4.41%, 4.21%	3.08%, 4.12%
THD of load voltage during voltage harmonic distortion in source voltage	4.59%	3.51%
Sampling time	10 μs, fixed step	10 μs, fixed step

Table 2. DC link voltage dynamics with proposed and conventional control algorithms

Parameters	SRFT based control algorithm	Proposed adaptive LMS based control algorithm
Rise time, T_r (sec)	0.12 s	0.2 s
Settling time, T_r (sec)	0.32 s	0.23 s
Peak overshoot, M_p (%)	10.18 %	1.96 %

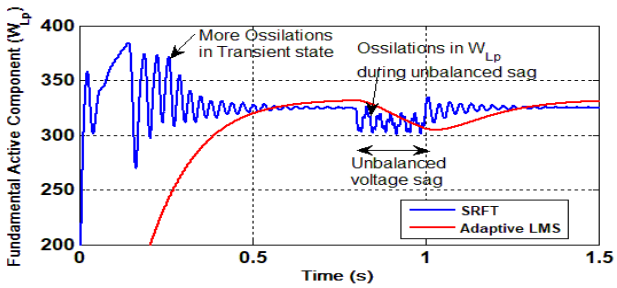


Figure 12. (a) Extraction of fundamental component of source voltage for SRFT and adaptive LMS base control (W_{Lp})

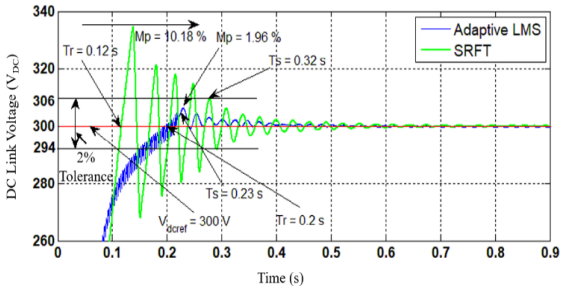


Figure 12. (b) Dynamics of DC bus voltage using SRFT and adaptive LMS based control

5. Experimentation Verification Using Digital Real-Time simulator

To check the effectiveness of the proposed control algorithm for DVR, a real-time digital simulator is used. A photograph of the experimental set-up is demonstrated in Figure 7. A computer having OPAL RT lab software is utilized to check the real-time performance of DVR. OPAL-RT (Real-time digital simulator) consists of X11SSM-E-F-O Supermicro Server Motherboard, Intel Socket H4 LGA-1155 µTAX and Intel Xeon 3.5GHz processor operating under RT-Lab environment. There are 32 digital I/O and 16 Analog I/O ports available in OPAL-RT. DVR control algorithm and power circuit components such as programmable voltage source, injection transformer, IGBT based VSC, critical load and ripple filter, etc. are implemented in OPAL-RT. In practical applications, power circuit components will be replaced by an actual voltage source, injection transformer, IGBT based VSC, critical load and ripple filter, etc. but the control algorithm will remain same to provide the control pulses for the VSC of DVR in real time. A digital storage oscilloscope (Tektronics, TDS 2014C) is used to show the OPAL RT waveforms in real time and fluke power quality analyzer (FLUKE,435-II) is used to record the harmonic spectrum of PCC voltage as well as load voltage.

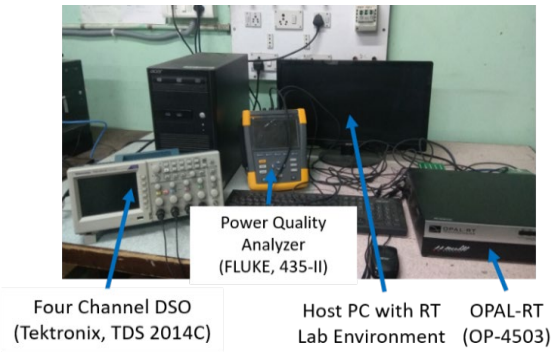


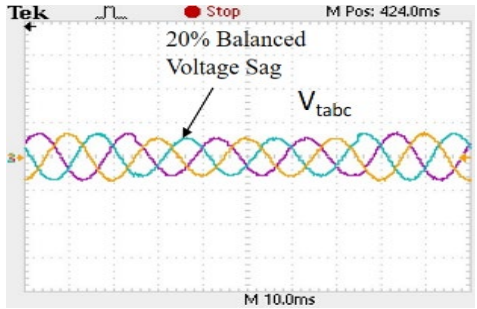
Figure 13. Experimental set-up

The performance of DVR is tested under various types of voltage quality issues as,

1. 20% balanced voltage sag/swell compensation
2. 20% unbalanced voltage sag/swell compensation
3. Voltage harmonic distortion compensation

Figures 14(a)-(d) and 15(a)-(d) show the performance of DVR under balanced voltage sag/swell compensation respectively. Figures 14(a) and 15(a) show the PCC voltage during balanced sag/swell condition. A balanced voltage sag/swell of 20% magnitude is introduced in the supply side for the duration of 3 cycles. Figures 14(b) and 15(b) show the injected voltage by DVR during these disturbances. To show the proper compensation, phase 'a' parameters such as PCC voltage, injected voltage and load voltage are shown in Figures 14(c) and 15(c). DC link voltages in both cases during the steady state as well as compensation are also shown in Figures

14(c) and 15(c). DC link voltage is within the desired limit which shows the excellent working of DC link voltage PI controller. Figures 14(d) and 15(d) show the waveforms of compensated load voltage during balanced voltage sag/swell disturbances. The real-time waveforms prove the effectiveness of the proposed control algorithm.



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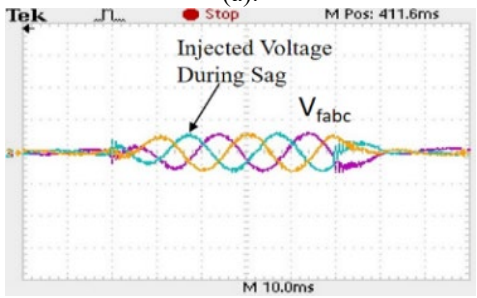

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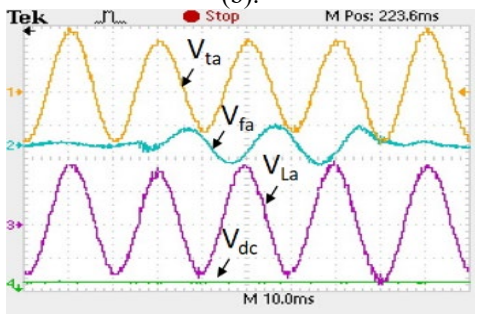

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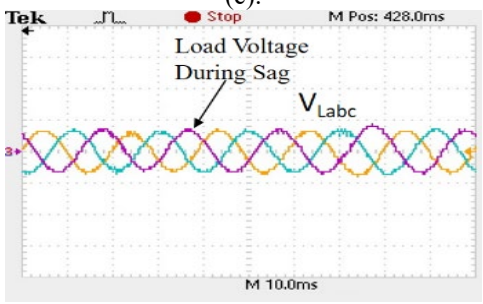
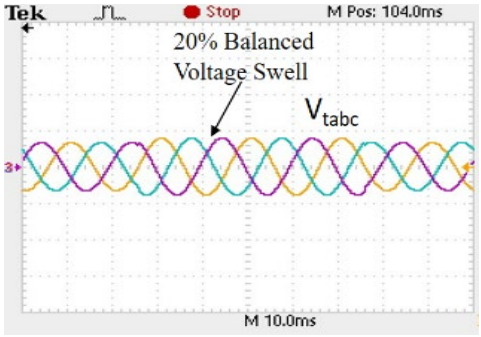


(d)

Figure 14. Experimentation results during balanced voltage sag condition (a) Three phase PCC voltages during 20% balanced voltage sag (b) Three phase injected voltages (c) Phase-a PCC voltage, injected voltage, load voltage and DC link voltage (d) Three phase undistorted load voltages



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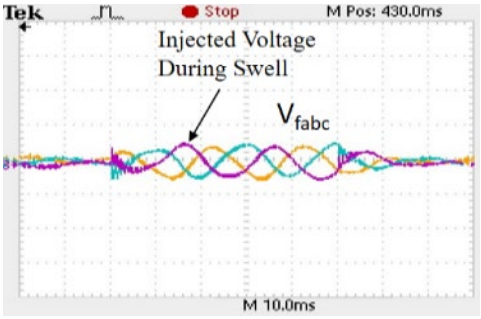

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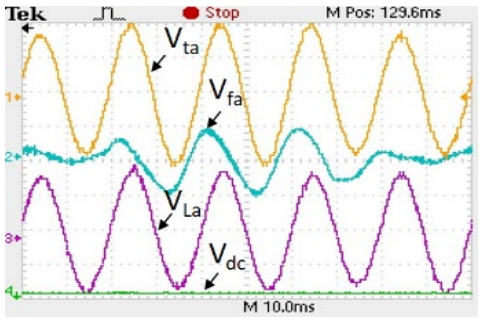

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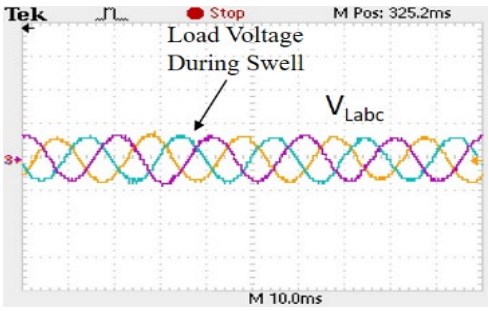
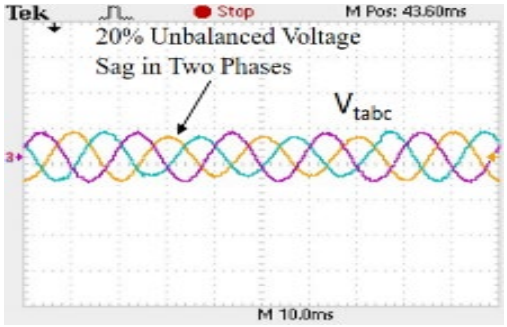


(d).

Figure 15. Experimentation results during balanced voltage swell condition (a) Three phase PCC voltages during 20% balanced voltage swell (b) Three phase injected voltages (c) Phase-a PCC voltage, injected voltage, load voltage and DC link voltage (d) Three phase undistorted load voltages

Figures 16(a)-(d) and 17(a)-(d) show the performance of DVR under unbalanced sag/swell compensation respectively. Figures 16(a) and 17(a) show the PCC voltage during unbalanced sag/swell condition. An unbalanced voltage sag/swell of 20% magnitude is introduced in the two phases of supply for the duration of 3 cycles. Figures 16(b) and 17(b) show the injected voltage by DVR during these unbalancing conditions. Figures 16(c) and 17(c) show the waveforms of compensated load voltage during unbalanced voltage sag/swell disturbances. The real-time waveforms prove the effectiveness of the proposed control algorithm.



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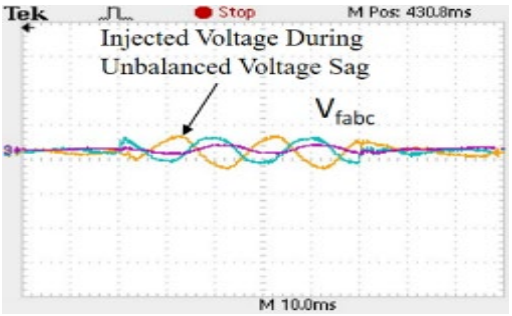

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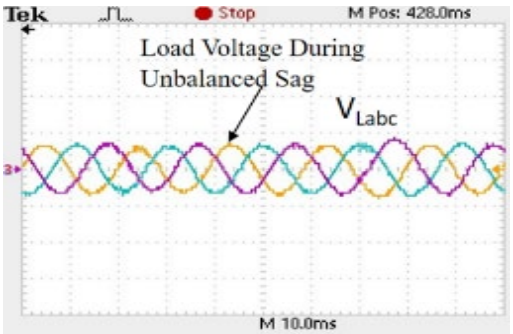
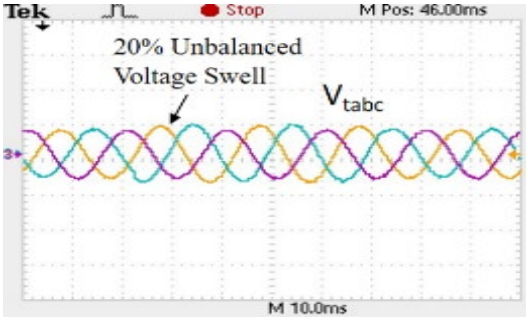


(c).

Figure 16. Experimentation results during unbalanced voltage sag condition (a) Three phase PCC voltages during 20% unbalanced voltage sag in two phases (b) Three phase injected voltages (c) Three phase undistorted load voltages



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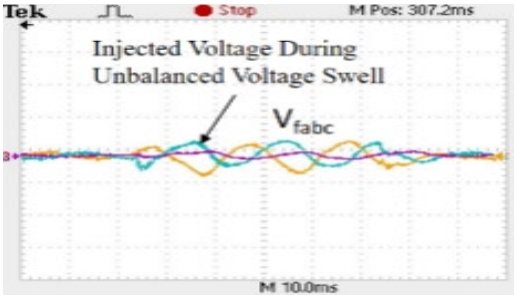

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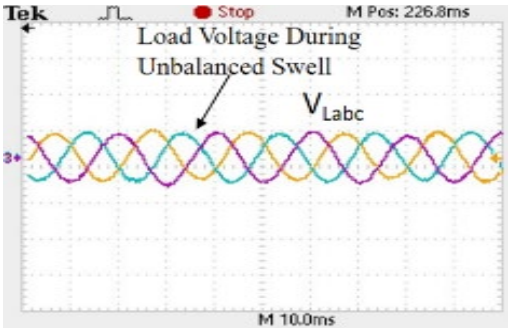
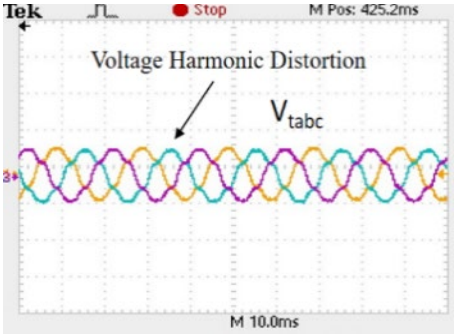


Figure 17. Experimentation results during unbalanced swell condition (a) Three phase PCC voltages during 20% unbalanced voltage swell in two phases (b) Three phase injected voltages (c) Three phase undistorted load voltages

Figure 18(a)-(d) show the performance of DVR under voltage harmonic distortion at PCC. Figure 18(a) shows the PCC voltage during voltage harmonic distortion. A three-phase programmable voltage source is used to inject the voltage harmonics at the source side. Figure 18(b) shows the DVR injected voltage to cancel out these harmonics at PCC. To show the proper compensation, phase 'a' parameters such as PCC voltage, injected voltage and load voltage are shown in Figure 18(c). DC link voltages during the steady state as well as compensation are also shown in Figure 18(c). DC link voltage is within the desired limit. Figure 18(d) shows the waveforms of compensated load voltage during voltage harmonic distortion. The load is at its desired value and undistorted. Subplots 1 to 4 of Figure 19 show the PCC voltage, the harmonic spectrum of PCC voltage, load voltage and harmonic spectrum of load voltage. It is also observed from the results that the total harmonic distortion (THD) in load voltage is within the limit (i.e., THD < 5%) according to IEEE-519 standard.



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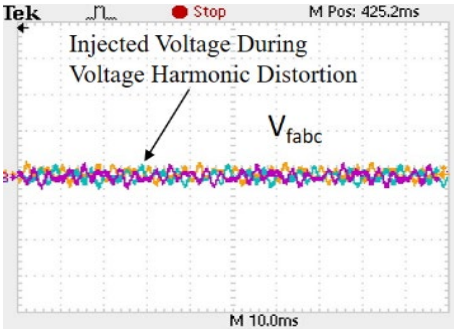

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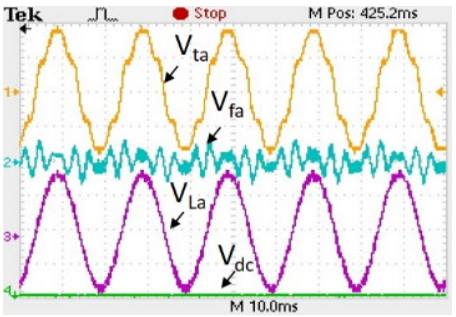

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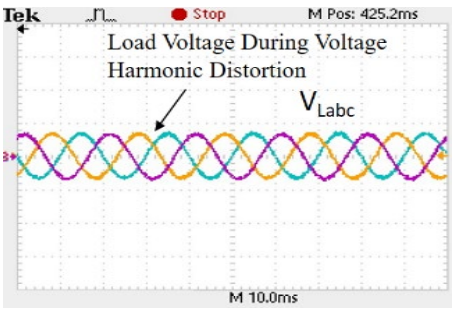
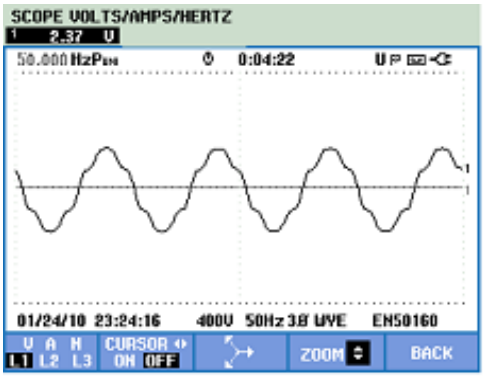


(d).

Figure 18. Experimentation results during voltage harmonic distortion (a) Three phase PCC voltages during voltage harmonic distortion (b) Three phase injected voltages (c) Phase-a PCC voltage, injected voltage, load voltage and DC link voltage (d) Three phase undistorted load voltages



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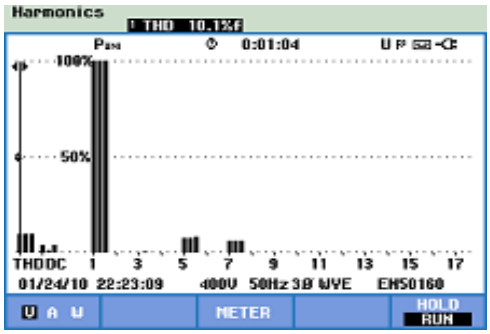
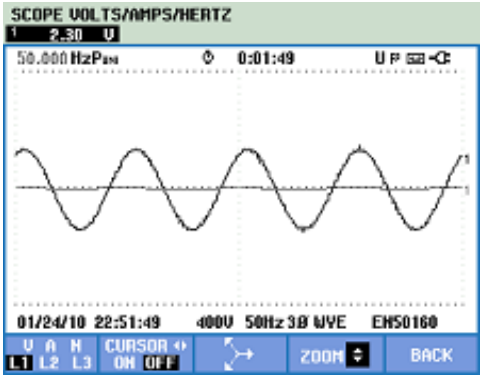


(b).



(c).

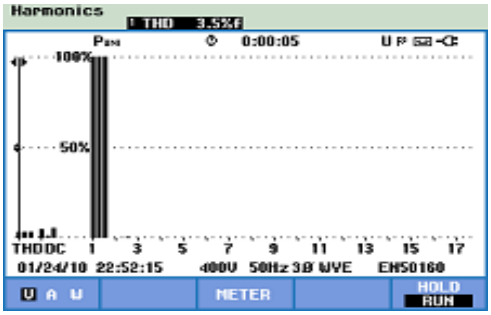


Figure 19. (a) Source voltage (b) THD spectrum of source voltage (c) Load voltage (d) THD spectrum of the load voltage

6. Conclusion

The main aim of this research work is to investigate the performance of DVR for providing clean and reliable power supply to the consumer load in case of voltage quality issues such as balanced voltage sag/swell, unbalanced voltage sag/swell, voltage harmonic distortion and combination of all in the supply side. The validation of the adopted control algorithm (Adaptive LMS) has been done by using simulation studies as well as real-time simulation. The adopted control algorithm is dynamically mitigating the above-discussed voltage quality issues and it is perfectly extracting the reference load voltages from the distorted PCC voltages. This control algorithm is very fast in nature and providing the desired results within a short time. This control strategy is capable enough to compensate short as well as long duration voltage disturbances at source side but it is not suitable for high depth voltage sags. The designing of main system parameters such as IGBT based VSC, three-phase injection transformer, ripple filter and AC side inductance has been given in detail. It has been investigated that the control algorithm is very easy to implement and work properly for various types of voltage related power quality problems at the source side.

appendix

System Parameters: Source parameter = 415 V, 50 Hz; Injection transformer rating = 6.3 KVA, 70/150 V; DC link voltage and capacitance = 300 V, 4700 μF , AC side inductance = 4 mH; Switching frequency = 10 kHz, Ripple filter: R_r = 2Ω, C_r = 16 μF; 3-P load = 10 kVA, 0.8 pf (lagging); DC bus voltage low pass filter cutoff frequency = 10 Hz; AC voltage low pass filter cutoff frequency = 10 Hz; Adaptive constant for active as well as reactive component: μ = 0.0002; Sampling time = 10 μs, fixed step.

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