A Novel Reduced-Rule Fuzzy Logic Based Self-Supported Dynamic Voltage Restorer for Mitigating Diverse Power Quality Problems

Shubhendra Pratap Singh[1], Abdul Hamid Bhat[1], and Arfat Firdous[2]

[1]Department of Electrical Engineering, National Institute of Technology Srinagar, Kashmir, India
[2]Department of Physics, Islamia College of Science & Commerce Srinagar, Kashmir, India

Abstract: For shielding voltage sensitive loads from diverse power quality problems (Voltage harmonic distortion and voltage sag/swell) a wide variety of custom power devices are used. Dynamic voltage restorer (DVR) is one of the important custom power device presently used for mitigation of above mentioned power quality problems. In this paper, reduced-rule fuzzy logic controller based on synchronous reference frame theory for controlling of self-supported dynamic voltage restorer (DVR) is proposed. As a result of the proposed controller, the mathematical model of plant is not at all needed and the control signals required by the DVR are thoroughly provided during various types of power quality problems at the source side. The performance of this technique is better than the other existing techniques and it is very simple to implement, less complex, very flexible and robust in nature. For the same system parameters, the fuzzy logic based controller uses the less amount of reactive power to mitigate the various disturbances at source side compared to PI based controller, which results into reduced rating of IGBTs and consequently leading to lowering of the overall cost. DVR is simulated for mitigation of various power quality problems (voltage harmonic distortion, balanced voltage sag/swell, unbalanced voltage sag/swell, balanced voltage sag/swell with harmonic distortion and unbalanced voltage sag/swell with harmonic distortion) and the simulation results verified by experimental results are presented displaying the workability of proposed controller.

Index Terms: synchronous reference frame theory, voltage sag/swell, power quality, fuzzy logic controller, dynamic voltage restorer

1. Introduction

A number of power quality problems such as voltage sag, voltage swell, voltage unbalancing and voltage harmonic distortion reported in literature [1-4] due to the extensive use of power electronics devices, integration of renewable power sources such as wind and solar in the micro-grid and occasion of various types of faults on the distribution network. Many sensitive loads such as medical equipment, communication networks, semiconductor industries, computer loads etc are extremely sensitive towards the power quality problems. Thus the utility of custom power devices for the betterment of above mentioned power quality problems oversides. Basically three categories of custom power devices exist, which can be categories on their respective functionality. For the mitigation of current quality problems a shunt connected device called Distributed Static Synchronous Compensator (D-STATCOM) [5-6] is used. Whereas a series connected device namely DVR [8-9] is used for the rectification of voltage quality problems. Further on in certain situation where mitigation of both current and voltage quality is required unified power quality conditioner (UPQC) [7] is applied. DVR is connected between the load and supply via the injection transformer. It can protect the voltage sensitive loads by mitigating various power quality problems.

There are many types of DVR topologies discussed in the literature [10]. Many types of voltage injection methods [11] are discussed. In [12-18], various types of control strategies are discussed for controlling of DVR. Some of the famous control strategies are Adaline based fundamental extraction, space vector modulation, energy optimized control and synchronous reference frame theory.

Received: March 23rd, 2018. Accepted: March 11st, 2019
DOI: 10.15676/ijeei.2019.11.1.4

Singh et.al [11] have demonstrated and implemented the DVR based on a synchronous reference frame theory algorithm. In this paper, two PI controllers are used to maintain DC bus voltage constant as well as to keep load voltage at the reference value. To obtain the gain values of load voltage PI controller is really a difficult task. Moreover, the mathematical model of the plant is necessary to design this controller. Addition of some non-linearity in the system results into an increment in the computational time and makes the mathematical model of the plant a bit complex [19].

In the present work the PI controller concerned with the load voltage is replaced by the reduced-rule based fuzzy logic controller (FLC). There is no need for mathematical modeling of the plant which makes the system less complex, fast and suitable for various non- linearities in the system. In most of the fuzzy logic based algorithms [20-22], 7 membership functions are taken for error and derivative of error thus the total number of rules become equals to 49 (7*7). But in this paper, only 3 membership functions are taken consequently the number of rules are reduced to only 9 (3*3). There is a huge reduction in the number of rules achieved by the proposed fuzzy logic controller which makes the system faster and reduces the computational burden of the system. FLC deals with non-linear plant with little or no need for prior information of plant. An intelligent controller such as reduced-rule FLC proposed and implemented in this paper is not only capable of providing superior control for DVR over a wide range of operating condition but it is also able to reduce the control effort exerted by the device during large scale disturbances, which in-turn, leads to smaller MVA rating of the DVR and therefore less capital investment. Functioning of the proposed FLC controller depicts that it is very efficient to solve the various source side power quality issues like balanced voltage sag/swell, voltage harmonic distortion and unbalanced voltage sag/swell. In future, one can easily increase the number of rules considering the other problems of plant and the complexity of the controller will not increase rapidly.

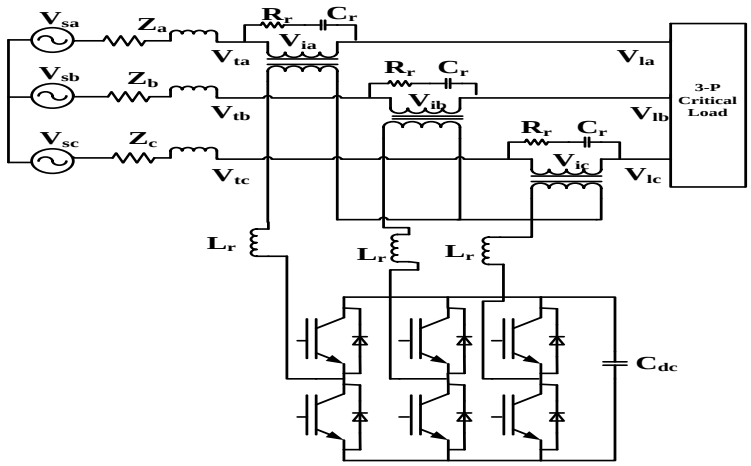


Figure 1. Schematic outline of self supported DVR

The main contributions of this paper are:

1. Reduced-rule based FLC is used to replace load voltage PI controller for better control purpose. The mathematical modeling of the plant is not required which makes the system less complex and robust in nature.
2. In this paper, only 3*3 rule base is taken in place of the conventional 7*7 rule base. In future, the number of rules can be increased considering other requirements of the plant which makes the system more flexible.
3. In this paper, comparison of fuzzy logic based and PI based controllers is done on the basis of their ability to mitigate source side power quality issues. Comparison shows that for same system parameters and same amount of disturbance, the fuzzy logic based controller requires

less control effort (i.e. uses the less amount of reactive power) compared to conventional PI based controller to mitigate these disturbances. This leads to less rating of IGBTs and therefore less cost for the devices. In addition, damping performance of fuzzy logic controller is better than the PI controller for addressing various disturbances at source side. The peak value of DC link voltage as well as settling time reduces by using fuzzy logic based controller as shown well in comparison.

4. Maintaining the stability of the system with many types of power quality issues like balanced voltage sag/swell, unbalanced voltage sag/swell, voltage harmonic distortion and balanced as well as unbalanced voltage sag/swell with harmonic distortion.

Figure 1 displays the fundamental block diagram of self-supported DVR. The main components of DVR are 3-Phase programmable voltage source, injection transformer, IGBT based VSC, ripple filter and DC link capacitance.

2. Modeling of Proposed Configuration

The proposed system for DVR comprises of 3-Phase programmable voltage source, insulated gate bipolar transistor (IGBT) based VSC, ripple filter, injection transformer and three-phase linear lagging load. The system components to be designed are ripple filter, AC side inductance and DC link capacitance. The data for the system are given in table 1.

A. Modeling of DC Link Capacitance

Proper functioning of VSC depends upon the appropriate value of DC link capacitance for better regularization of load voltage during various power quality problems. During sag as well as swell, DC side capacitor supplies or absorbs the power to maintain the load voltage constant. So the value of capacitance can be calculated as [23,24],

$$\frac{1}{2} \times C_{dc}(V_{dc}^2 - V_{dco}^2) = nST \quad (1)$$
$$\frac{1}{2} \times C_{dc}(300^2 - 297^2) = 0.1 \times 10000 \times .0042$$
$$C_{dc} \cong 4690\mu F$$

where, n=0.1 is the time taken by controller to regulate DC link voltage, S= 10 kVA shows the maximum load rating, T is the system time period, V_{dc}= 300V (DC link voltage) and V_{dco}= 297 shows the maximum change in DC link voltage during various power quality problems at source side. C_{dc} is calculated to be $4690\mu F$ and by further iteration, value of C_{dc} is taken to be $4700\mu F$(standard value).

Table 1. System parameters for simulation

System Parameters	Data
Line Voltage	415V, 50 Hz
Line impedance	Rs = 0.01Ω, Ls = 3.5mH
DC link voltage	VDC= 300V
DC link Capacitance	CDC= 4700 µF
Ripple Filter	Cr = 52 µF, Rr = 2Ω
AC Side Inductance	Lr = 2mH
Injection Transformer	10 KVA, 200V/300V
PWM switching frequency	fs = 10 kHz
Load	0.8pf lagging, 10KVA

B. Modeling of Ripple Filter

VSC switching frequency is used to design ripple filter [24-26]. Basically, ripple filter is designed to address the switching harmonics in VSC output voltage. It is a first order high pass filter whose RC time constant should be less than or equal to the time period at fundamental switching frequency as,

$$R_r \times C_r \leq T_s \tag{2}$$

Where, switching time $T_s = 1/f_s$ and f_s is the switching frequency (10 kHz), so the equation can be written as,

$$R_r \times C_r = \frac{1}{f_s} \tag{3}$$

Let us take R_s = 2 Ω then the value of C can be calculated as,

$$2 \times C_r \leq \frac{1}{10000}$$
$$C_r \cong 50\mu F$$

C. Modeling of AC Side Inductor

AC side inductor can be designed as [23-24],

$$L_r = \frac{\sqrt{3} m V_{dc}}{12\, h\, f_s\, \Delta i} \tag{4}$$
$$L_r = \frac{\sqrt{3}\times 1\times 300}{12\times 1.2\times 10000\times 1.8} \cong 2.0046\, mH$$

Where, V_{dc}= 300V (DC link voltage), m=1 (modulation index), h=1.2 (overloading factor), f_s= 10 kHz (switching frequency) and Δi = 2% of peak current. L_r is calculated to be 2.0046mH and by further iteration, the value of L_r is taken to be 2mH.

3. Proposed Control Algorithm

Figure 2 displays the fundamental block diagram of adopted control scheme. SRF theory with a fuzzy logic controller is adopted for the self-supported DVR. At the time of any disturbance, DVR insert the required voltage into the line via the injection transformer. Terminal voltages V_t are converted into rotating reference frame using parks transformation [11] as given in eq. (5). Low pass filters are a integral part of this algorithm. They are used to remove the harmonic and oscillatory component from the voltage component of d and q axis. The voltage components of d and q axis are given in eq. (6, 7).

$$\begin{bmatrix} V_{tq} \\ V_{td} \\ V_{t0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_{ta} \\ V_{tb} \\ V_{tc} \end{bmatrix} \tag{5}$$

$$V_d = V_{d,dc} + V_{d,har} \tag{6}$$
$$V_q = V_{q,dc} + V_{q,har} \tag{7}$$

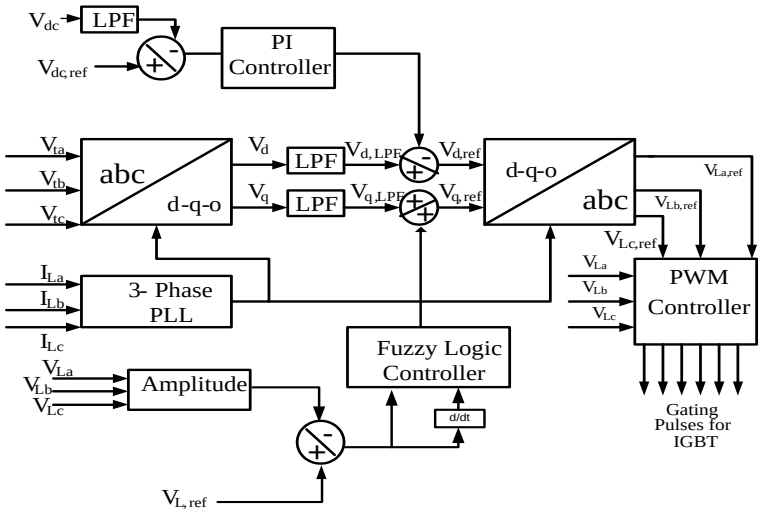


Figure 2. Proposed Control Algorithm

In the conventional SRF based algorithm [11], two PI controllers are used. One of the PI controllers is employed to regulate the DC link voltage and another PI controller is employed to regulate the load voltage during source side disturbances. Replacement of DC link voltage PI controller is not done in the work because DC link voltage is within limits by using this controller. The load voltage PI controller is replaced here due to fact that mathematical modeling of the plant is necessary to obtain the gain values of this controller.

A. PI-Based DC Bus Voltage Controller

The value of reference DC link voltage (V_{DC}) is equated with the value of sensed DC link voltage (V^*_{DC}) at k^{th} instant of time to generate the error signal as:

$$V_{e(k)} = V^*_{dc(k)} - V_{dc(k)} \tag{8}$$

To compensate this error ($V_{e(k)}$), a PI controller is used. The output of this controller at k^{th} instant of time as:

$$V_{cd(k)} = V_{cd(k-1)} + K_{pd}\left[V_{e(k)} - V_{e(k-1)}\right] + K_{id}V_{e(k)} \tag{9}$$

Here K_{pd} and K_{id} are the gains of PI controller. Subtraction of PI controller output and D-axis DC component gives the in-phase component of reference load voltage as given in eq. (10).

$$V^*_d = V_{d,dc} - V_{cd(k)} \tag{10}$$

B. Fuzzy Logic Based Load Voltage Controller

The error between the sensed DC link voltage and reference DC link voltage is processed by the fuzzy logic based controller. The advantage of this FLC is that there is no need for mathematical modeling of the plant. There is no need of mathematical model of plant in fuzzy logic controller; in this an expert knowledge is sufficient to make the logical rules. There are three steps in FLC and descriptions of steps are as:

1. FUZZIFICATION: -It is the process in which the error, change in error and output signal converts into fuzzified signals and different types of membership functions are used in order to represent these fuzzified signals in a fuzzy set. There are many types of membership functions as reported in literature such as triangular, trapezoidal, bell-shaped and Gaussian function [27] etc. In this paper, very simpler triangular membership functions are used. The

membership functions are triangular in shape but 50% overlap is not necessary here as shown in Figure 3. The prior knowledge of the plant is very necessary in order to design a more efficient membership function for better control purposes. The Sugeno type FLC is used for the output membership functions having singleton shape as shown in Figure 3. The linguistic variables represent output, error and derivative of error as zero error (ZE), negative big (NB), and positive big (PB). Only three membership functions are used which are sufficient to tackle all types of power quality problems at the source side that result into the reduced computational burden. Triangular membership function [28] cab be define as a function of vector x as shown in eq. (11).

2.

$$\Delta\,(x{:}\,a,b,c) = \begin{cases} \frac{x-a}{x-b} & if\ a \le x \le b \\ \frac{c-x}{c-b} & if\ b \le x \le c \\ 0, & otherwise \end{cases} \tag{11}$$

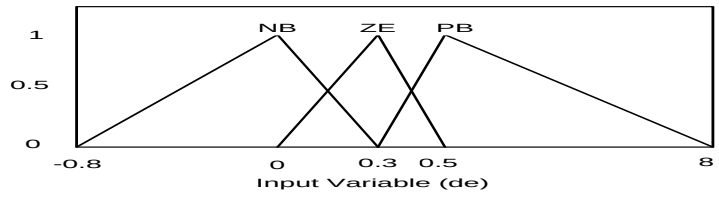
3. FUZZY RULE BASE:- Table 2 demonstrates the rule base used for obtaining the output of fuzzy logic controller. If-then rules define a fuzzy interface system (FIS) by connecting the input to output. Sugeno inference method [29] is very effective for obtaining the relation between its inputs and outputs.
4. DEFUZZIFICATION:- The output of FLC is in linguistic labels which have to change back into a crisp solution variables. Sugeno's wtaver is selected for defuzzification. Finally, the output of this FLC ($V_{cq(k)}$) is getting added to the DC voltage component of q axis to obtain the quadrature component of reference load voltages as given in eq. (12).

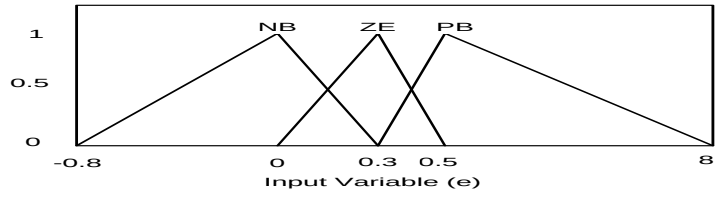
$$V_q^* = V_{q,dc} + V_{cq(k)} \tag{12}$$

C. Estimation of Reference Load Voltage

Reverse park transformation [11] is used to convert the in-phase component (V_d^*) and quadrature component (V_q^*) of reference load voltage into abc frame as represent in eq. (13). The SPWM (Sinusoidal pulse width modulation) controller is utilized for compensating the error between reference load voltage ($V_{La}^*, V_{Lb,}^* V_{Lc}^*$) and sensed load voltages (V_{La}, V_{Lb}, V_{Lc}) in order to get the gating pulses for VSC of DVR.

$$\begin{bmatrix} V_{La}^* \\ V_{Lb}^* \\ V_{Lc}^* \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} V_q^* \\ V_d^* \\ V_0^* \end{bmatrix} \tag{13}$$





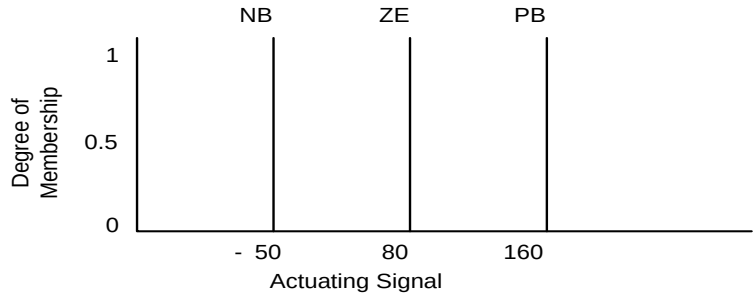


Figure 3. (a) Membership function for error e (b) Membership function for derivative of error de (c) Membership function for output

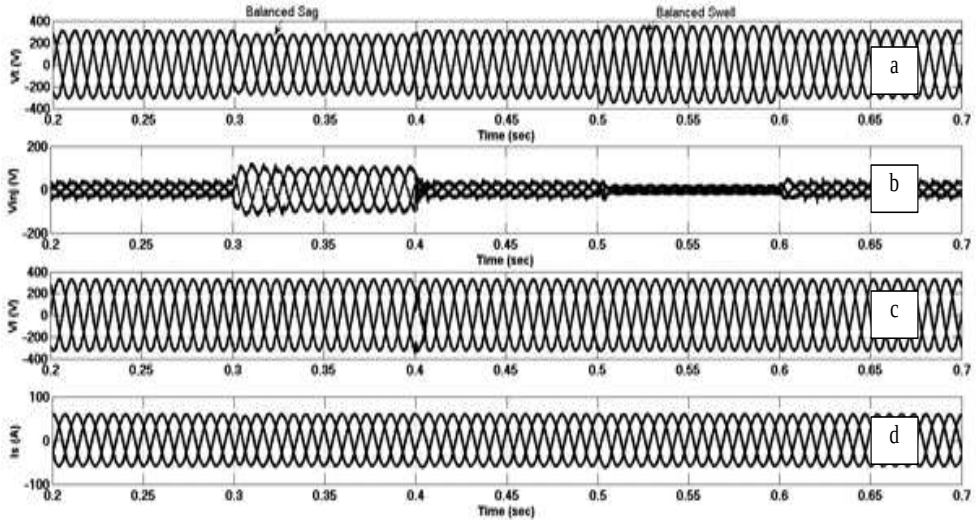
Table 2. Control rule base

de \ e	NB	ZE	PB
NB	NB	NB	ZE
ZE	NB	ZE	PB
PB	ZE	PB	PB

5. Performance Investigation

The DVR system is simulated, designed and modeled by using MATLAB/Simulink & SimPowerSystems environment. Moreover, the components of the system such as DC link capacitance, AC side inductance and ripple filter are designed in detail [23-26]. All the system parameters are given in table 1. The reference load voltages for VSC of DVR are generated from sensed load voltage (V_{La}, V_{Lb}, V_{Lc}), sensed source terminal voltage (V_{ta}, V_{tb}, V_{tc}) and load current (I_{La}, I_{Lb}, I_{Lc}). Performance of the designed system is simulated for distinct power quality issues at source side like balanced as well as unbalanced voltage sag/swell, voltage harmonics distortion, and balanced as well as unbalanced voltage sag/swell with harmonics distortion.

A. Performance under Balanced Voltage SAG/SWELL Condition



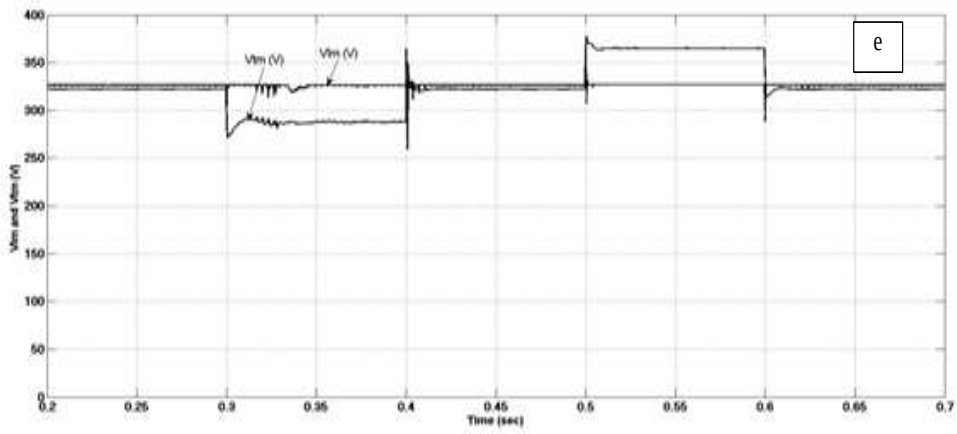


Figure 4. Waveforms during balanced voltage sag/swell condition (a) Source terminal voltage V_t (b) injected voltage V_{inj} (c) Load voltage V_L (d) Source current I_s (e) Amplitude of source and load voltage (V_{tm}, V_{lm})

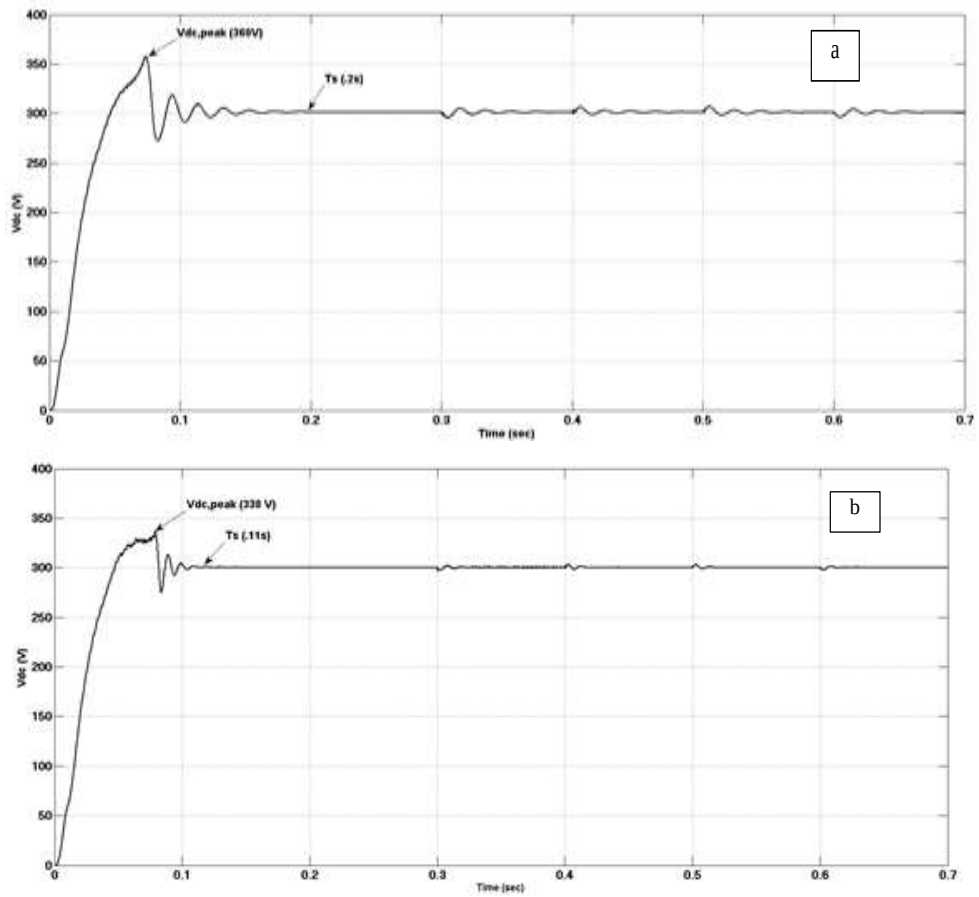


Figure 5. (a) DC bus voltage V_{dc} using PI controller (b) DC bus voltage V_{dc} using FLC controller

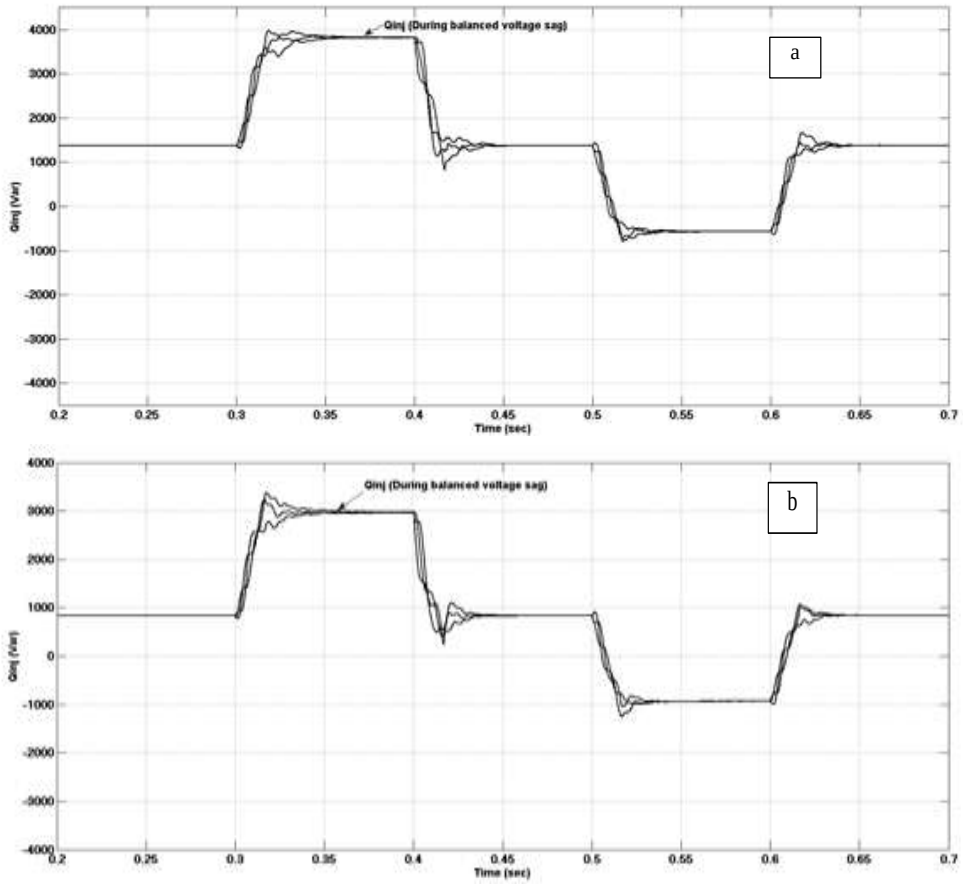
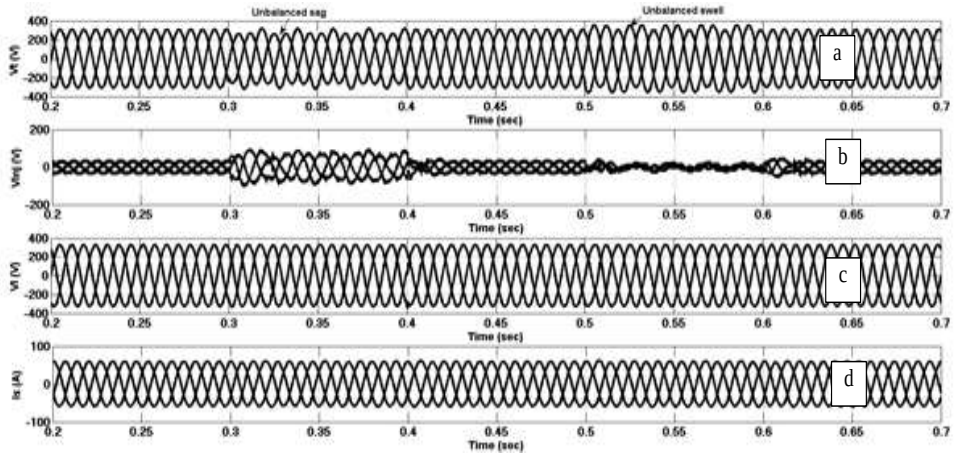


Figure 6 (a) Reactive power injection (Q_{Var}) using PI controller (b) Reactive power injection (Q_{Var}) using FLC controller

B. Performance under Unbalanced Voltage SAG/SWELL Condition



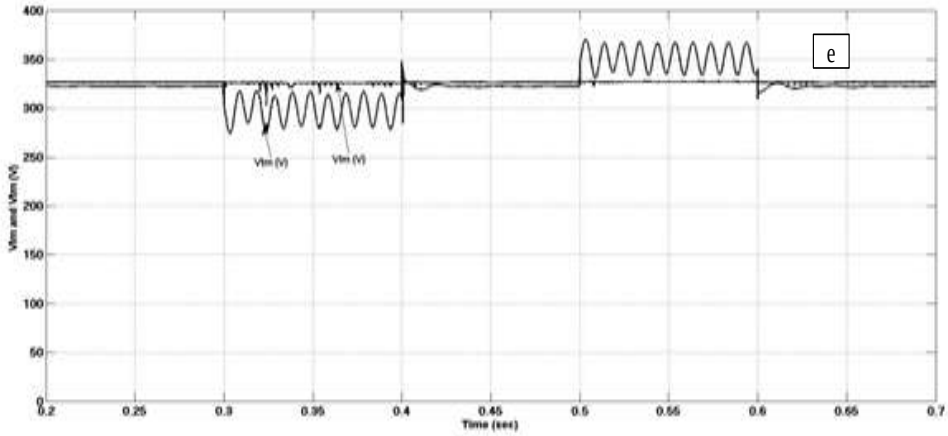


Figure 7. Waveforms during unbalanced voltage sag/swell condition (a) Source terminal voltage V_t (b) injected voltage V_{inj} (c) Load voltage V_L (d) Source current I_s (e) Amplitude of source and load voltage (V_{tm}, V_{lm})

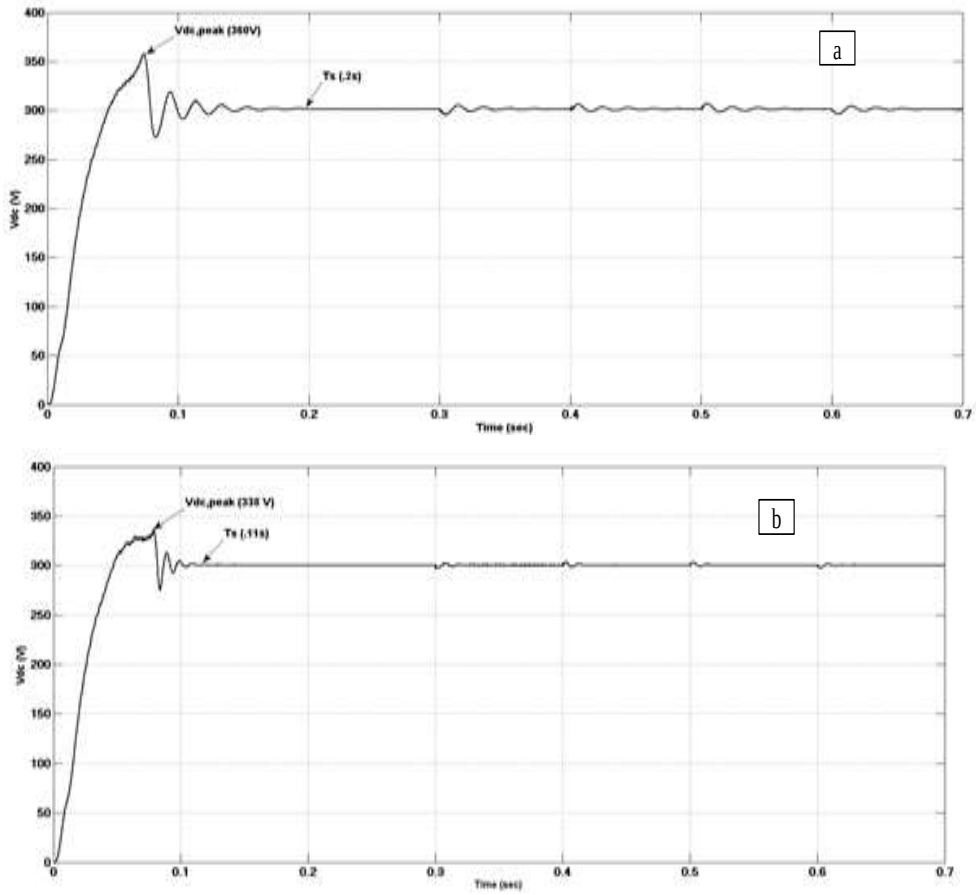


Figure 8. (a) DC bus voltage V_{dc} using PI controller
(b) DC bus voltage V_{dc} using FLC controller

Unbalanced voltage sag (15% sag in phase A and 20% sag in phase B) is introduced in the system at 0.3s and unbalanced voltage swell (15% swell in phase A and 20% swell in phase B) is introduced in the system at 0.5s for the duration of 5 cycles. At the time of any disturbance (unbalanced voltage sag/swell), DVR will use the reactive power to regulate the load voltage. Source terminal voltage V_t, DVR injected voltage V_{inj}, load voltage V_L, source current I_s and amplitude of source as well as load voltage (V_{tm}, V_{lm}) are displays in Figure 7. Figure 8 reveals that there are less oscillations and less overshoot in the DC link voltage observed in the fuzzy logic based DVR. Reactive power injected during unbalanced voltage sag by each controller shown in Figure 9.

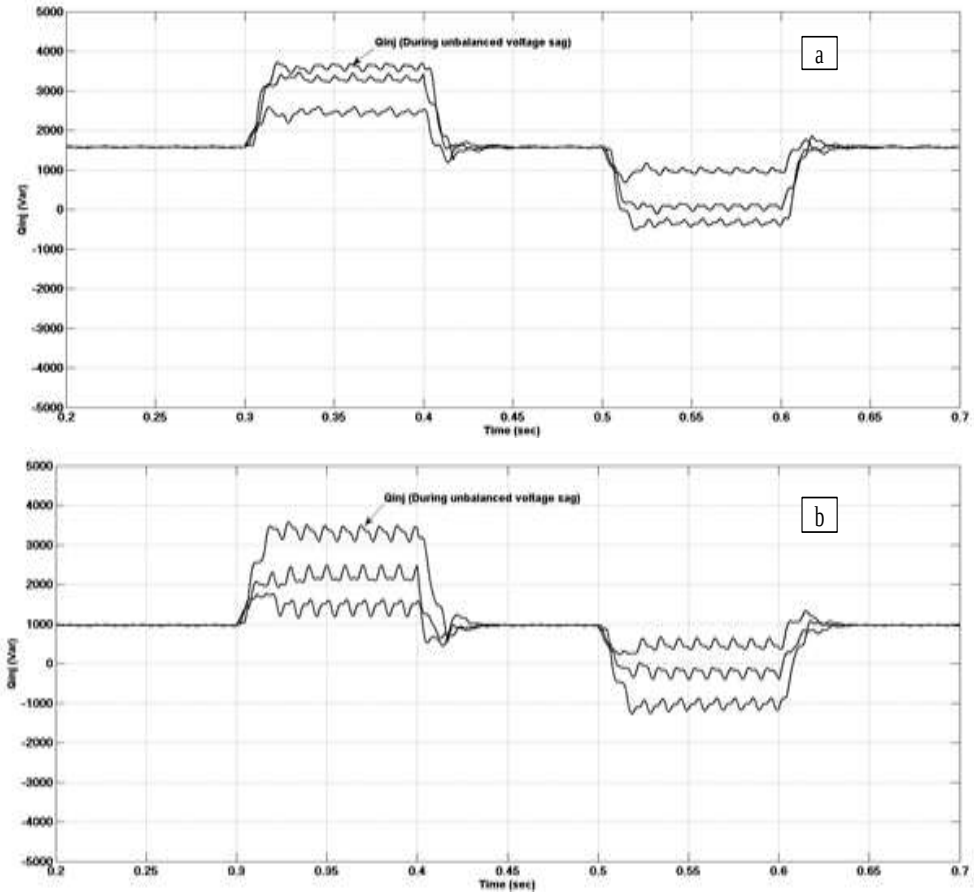


Figure 9 (a) Reactive power injection (Q_{Var}) using PI controller (b) Reactive power injection (Q_{Var}) using FLC controller

C. Performance under Voltage Harmonic Distortion

5th (20%) and 7th (14%) harmonics distortion is inserted in the supply voltage by the programmable voltage source in all the three phases. DVR injects proper amount of compensation voltage to regulate the load voltage and make it sinusoidal in nature. Source terminal voltage V_t, DVR injected voltage V_{inj}, load voltage V_L, source current I_s, DC bus voltage V_{dc} and amplitude of source and load voltage (V_{tm}, V_{lm}) are displays in Figure 10. The total harmonic distortion (THD) is 26.80% in the supply voltage (Figure 11). THD in load voltage is only 1.65% (Figure 12) and only 0.46% (Figure 13) in the source current after the excellent performance by DVR.

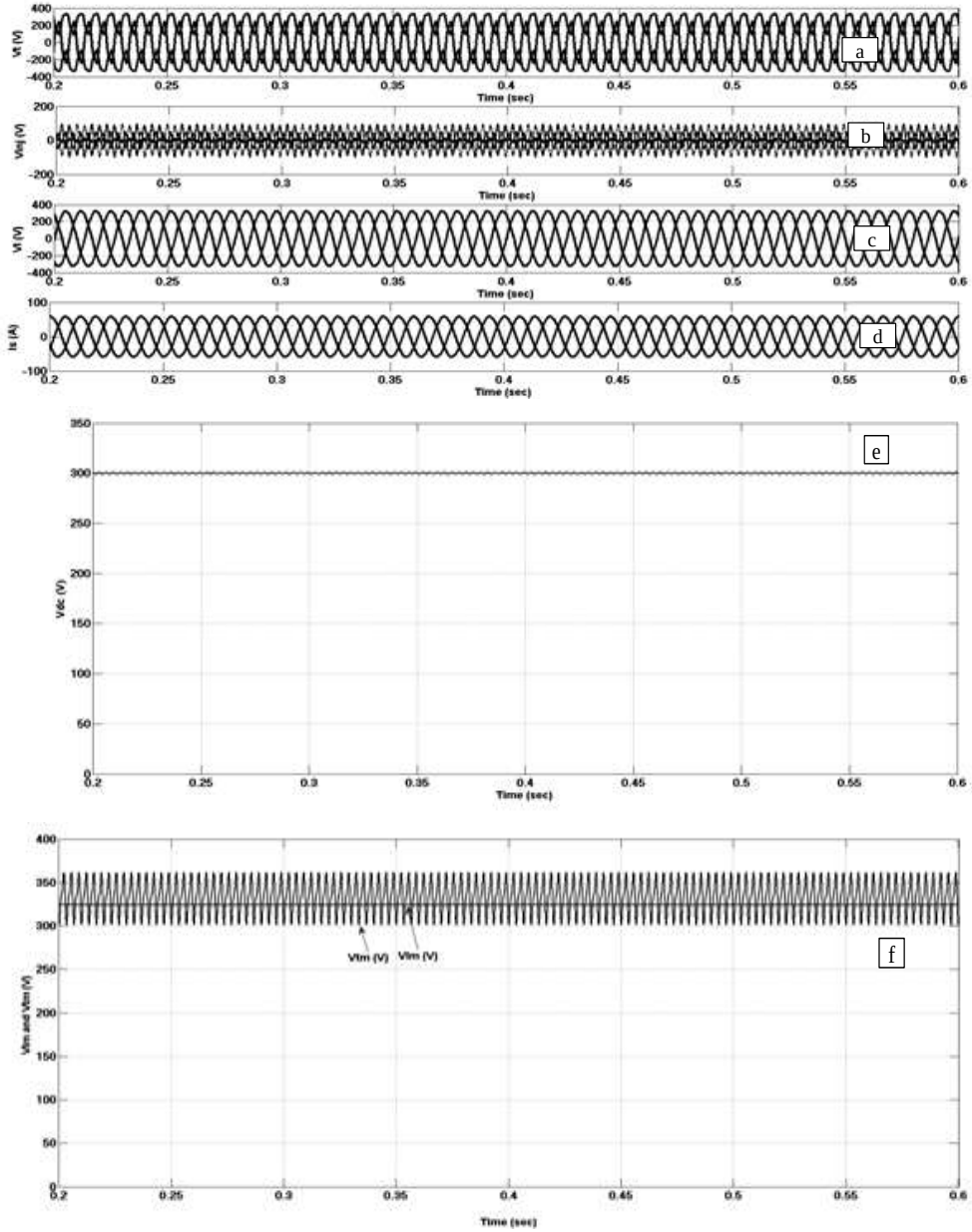
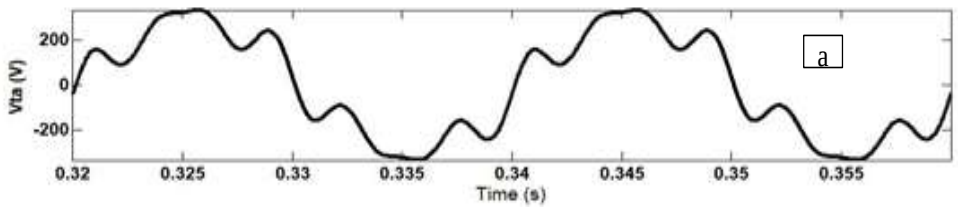


Figure 10. Waveforms during voltage harmonic distortion (a) Source terminal voltage V_t (b) injected voltage V_{inj} (c) Load voltage V_L (d) Source current I_s (e) DC bus voltage V_{dc} (f) Amplitude of source and load voltage (V_{tm}, V_{lm})



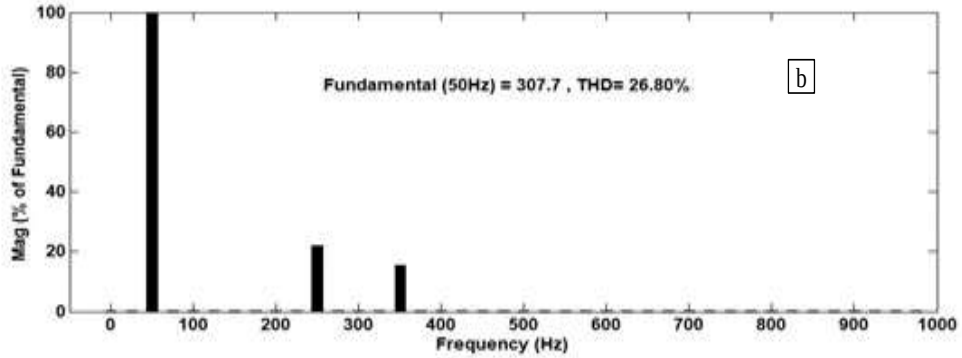


Figure 11. (a) Source terminal voltage (b) Harmonic spectrum

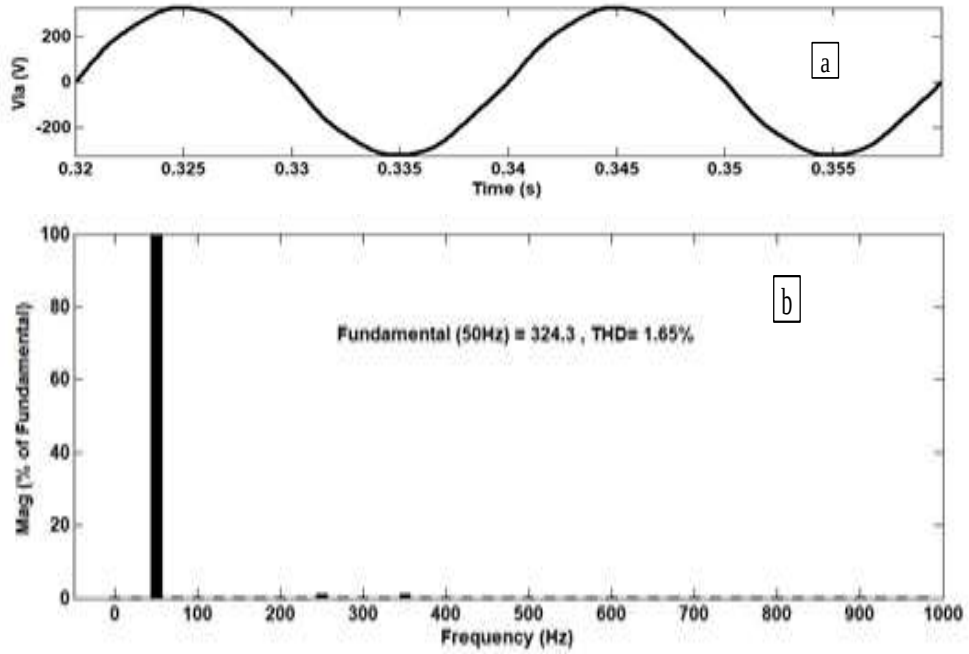
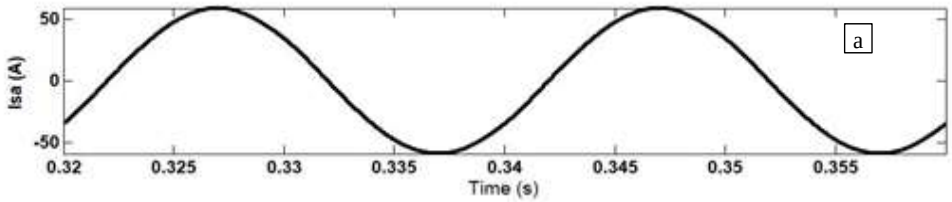


Figure 12. (a) Load voltage (b) Harmonic spectrum



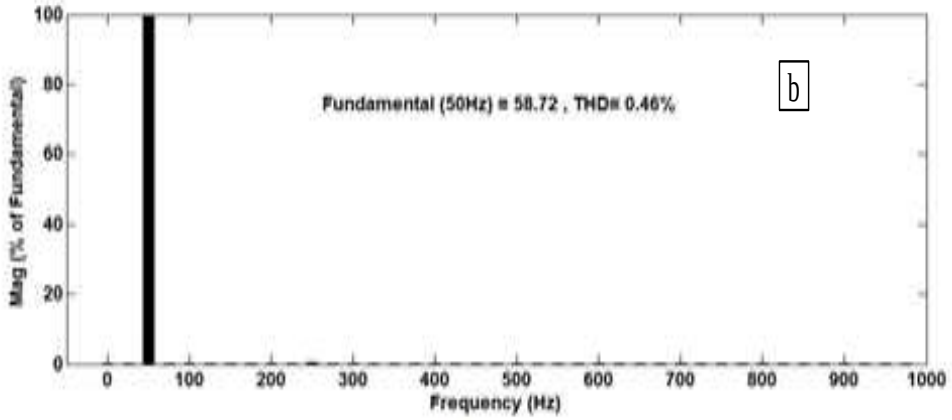


Figure 13. (a) Source current (b) Harmonic spectrum

D. Performance under Balanced Voltage SAG/SWELL with Harmonic Distortion

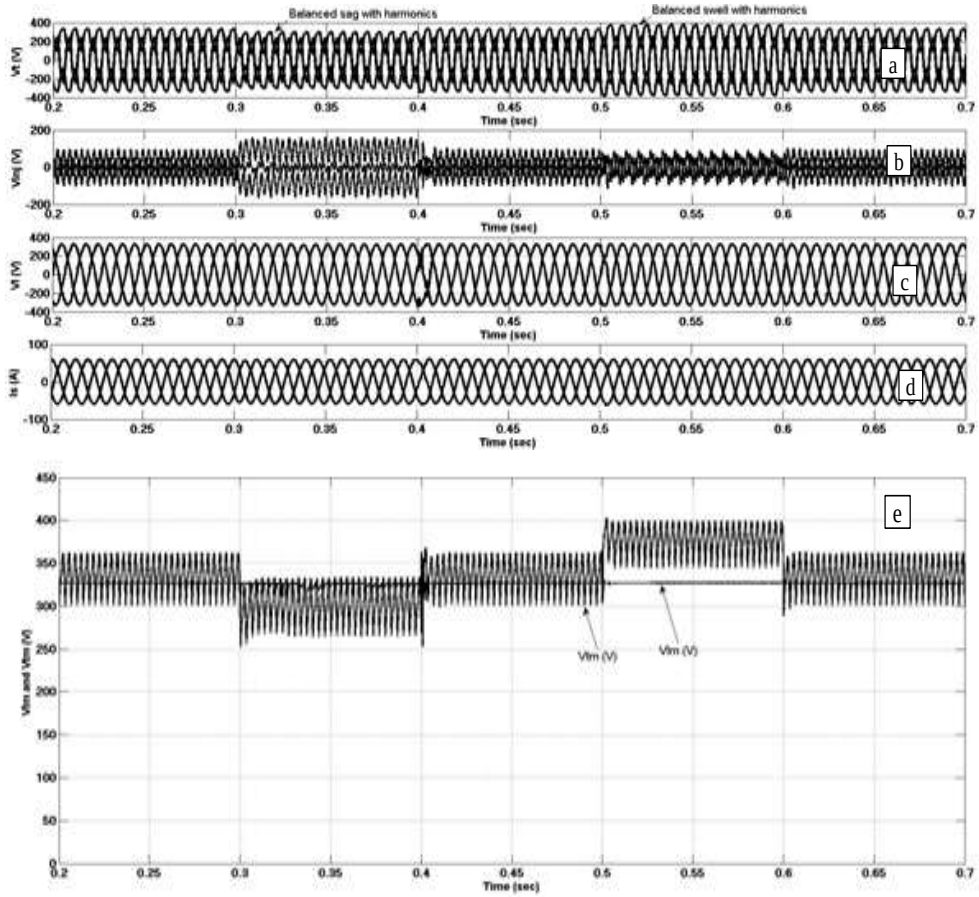


Figure 14. Waveforms during balanced voltage sag and balanced voltage swell with harmonic distortion (a) Source terminal voltage V_t (b) injected voltage V_{inj} (c) Load voltage V_L (d) Source current I_s (e) Amplitude of source and load voltage (V_{tm}, V_{lm})

Balanced voltage sag (15% of phase voltage) is introduced in the system at 0.3s and balanced voltage swell (15% of phase voltage) is introduced in the system at 0.5s for the duration of 5 cycles and also the 5th (20%) as well as 7th (14%) harmonics distortion is inserted in the supply voltage by the programmable voltage source in all the three phases. At the time of any disturbance (Voltage sag/swell with harmonic distortion), DVR will use the reactive power to maintain the load voltage constant and sinusoidal in nature. Source terminal voltage V_t, DVR injected voltage V_{inj}, load voltage V_L, source current I_s and amplitude of source and load voltage (V_{tm}, V_{lm}) are shown in Figure 14. Figure 15 reveals that there are less oscillations and less overshoot in the DC link voltage observed in the fuzzy logic based DVR. Reactive power injected during balanced voltage sag with harmonics by each controller shown in Figure 16. The total harmonic distortion (THD) is 30.16% in the supply voltage (V_{ta}) (Figure 17). THD in load voltage (V_{la}) is only 1.39% (Figure 18) and only 0.46% (Figure 19) in the source current after the excellent performance by DVR.

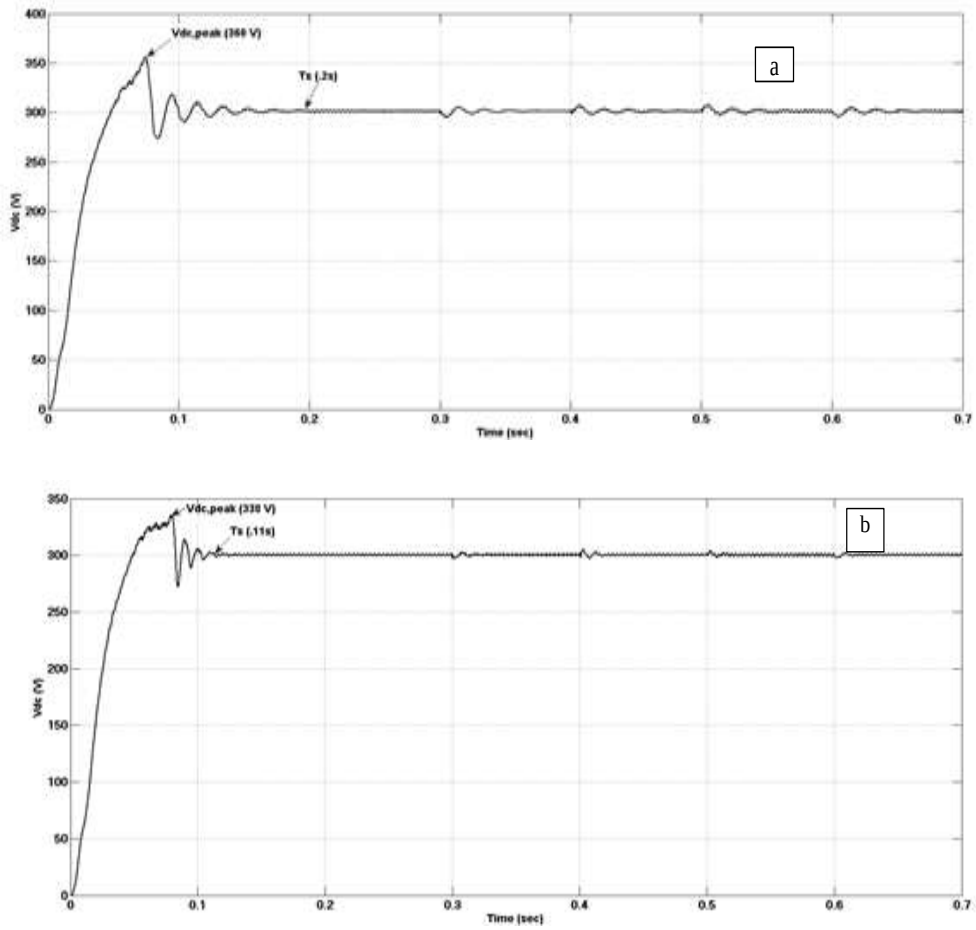


Figure 15. (a) DC bus voltage V_{dc} using PI controller
(b) DC bus voltage V_{dc} using FLC controller

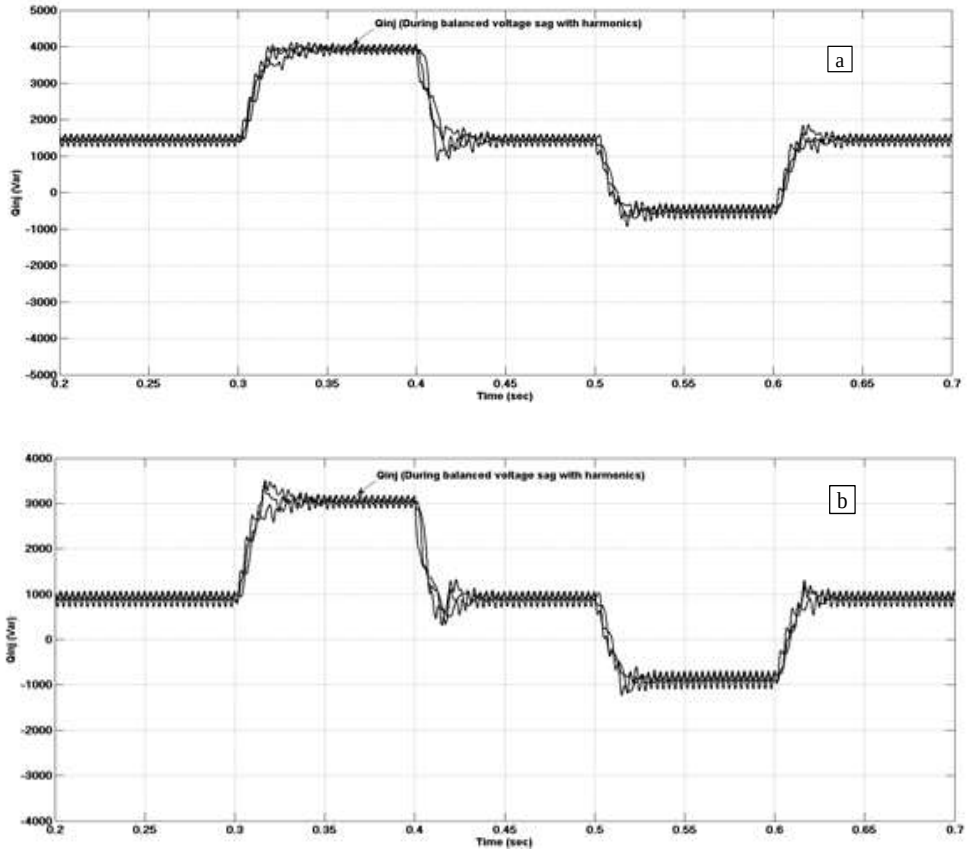


Figure 16 (a) Reactive power injection (Q_{Var}) using PI controller (b) Reactive power injection (Q_{Var}) using FLC controller

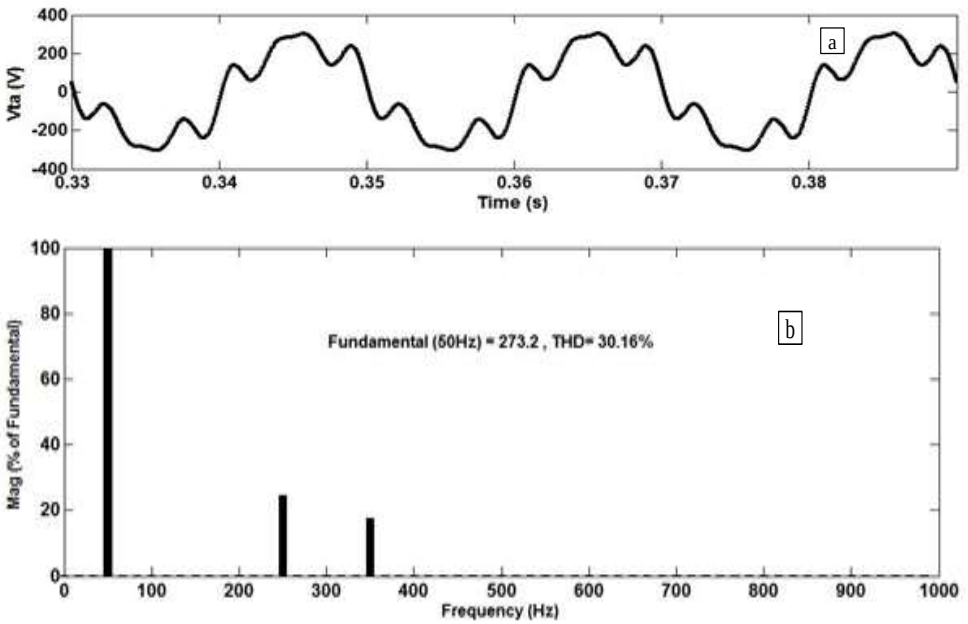


Figure 17. (a) Source terminal voltage (b) Harmonic spectrum

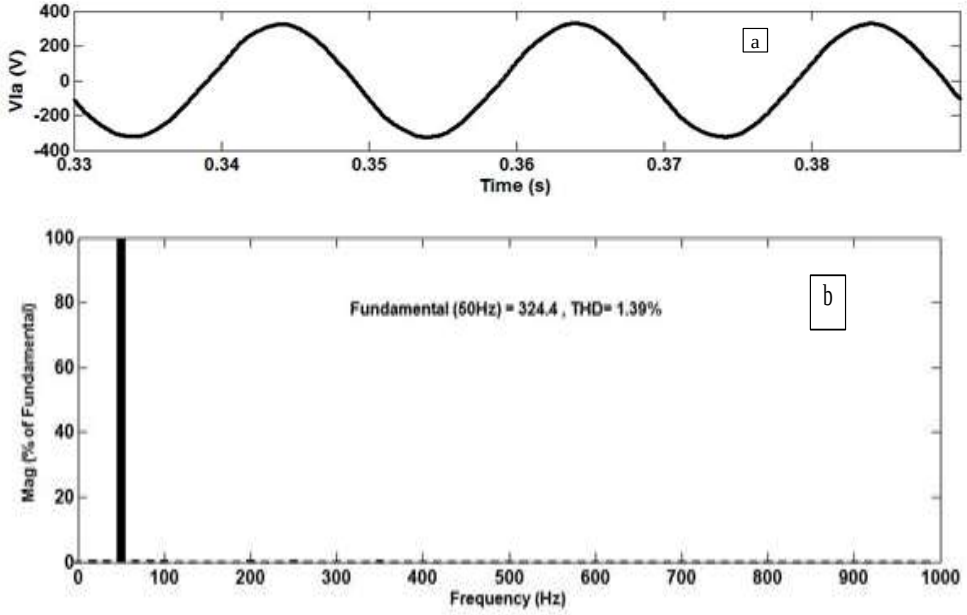


Figure 18. (a) Load voltage (b) Harmonic spectrum

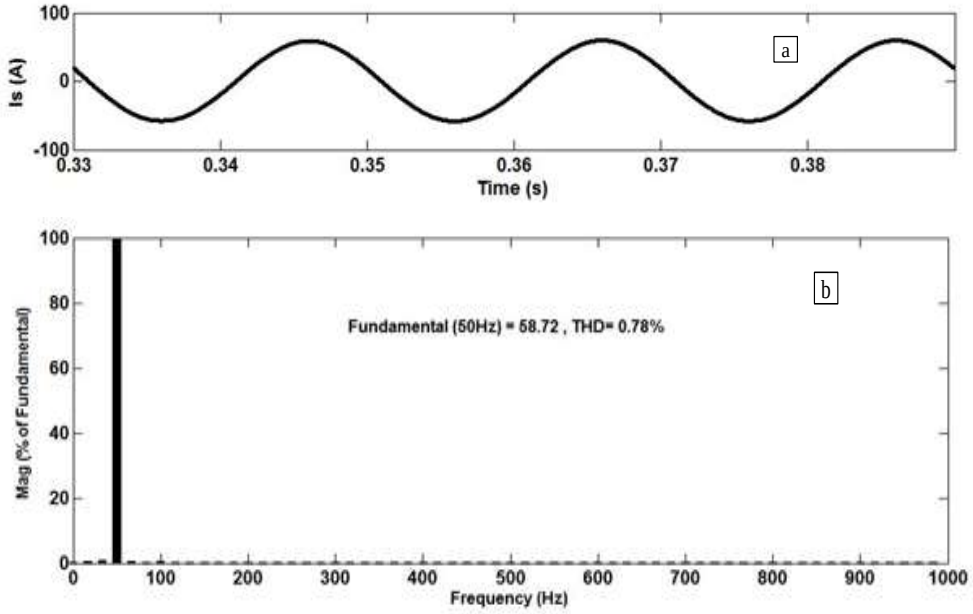


Figure 19. (a) Source current (b) Harmonic spectrum

E. *Performance under Unbalanced Voltage SAG/SWELL with Harmonic Distortion*

An unbalanced voltage sag (15% sag in phase A and 20% sag in phase B) is introduced in the system at 0.3s and unbalanced voltage swell (15% swell in phase A and 20% swell in phase B) is introduced in the system at 0.5s for the duration of 5 cycles and also the 5th (20%) as well as 7th (14%) harmonics distortion is inserted in the supply voltage by the programmable voltage source in all the three phases. At the time of any disturbance (Unvoltage sag/swell with harmonic

distortion), DVR will use the reactive power to maintain the load voltage constant and sinusoidal in nature. Source terminal voltage V_t, DVR injected voltage V_{inj}, load voltage V_L, source current I_s and amplitude of source and load voltage (V_{tm}, V_{lm}) are displays in Figure 20. Figure 21 reveals that there are less oscillations and less overshoot in the DC link voltage observed in the fuzzy logic based DVR. Reactive power injected during unbalanced voltage sag with harmonics by each controller shown in Figure 22. The total harmonic distortion (THD) is 26.03% in the supply voltage (V_{ta}) (Figure 23). THD in load voltage (V_{la}) is only 3.25% (Figure 24) and only 2% (Figure 25) in the source current after the excellent performance by DVR.

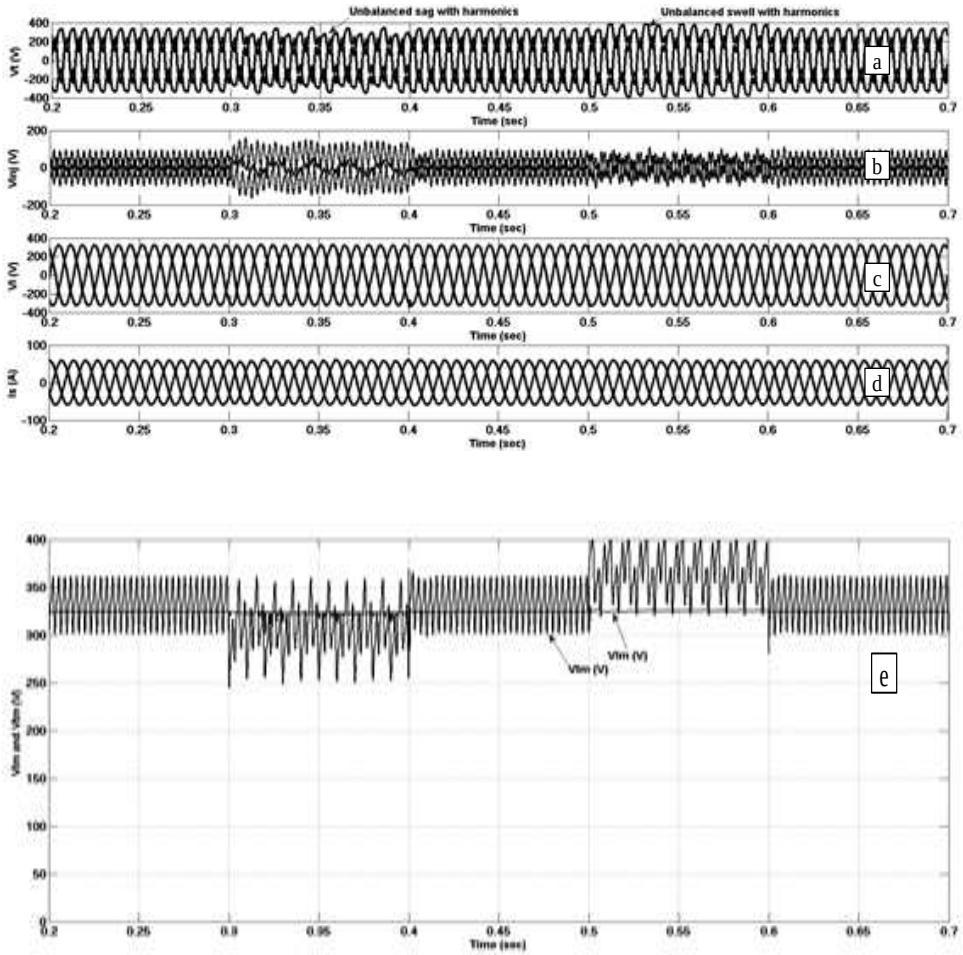


Figure 20. Waveforms during unbalanced voltage sag and unbalanced voltage swell with harmonic distortion (a) Source terminal voltage V_t (b) injected voltage V_{inj} (c) Load voltage V_L (d) Source current I_s (e) Amplitude of source and load voltage (V_{tm}, V_{lm})

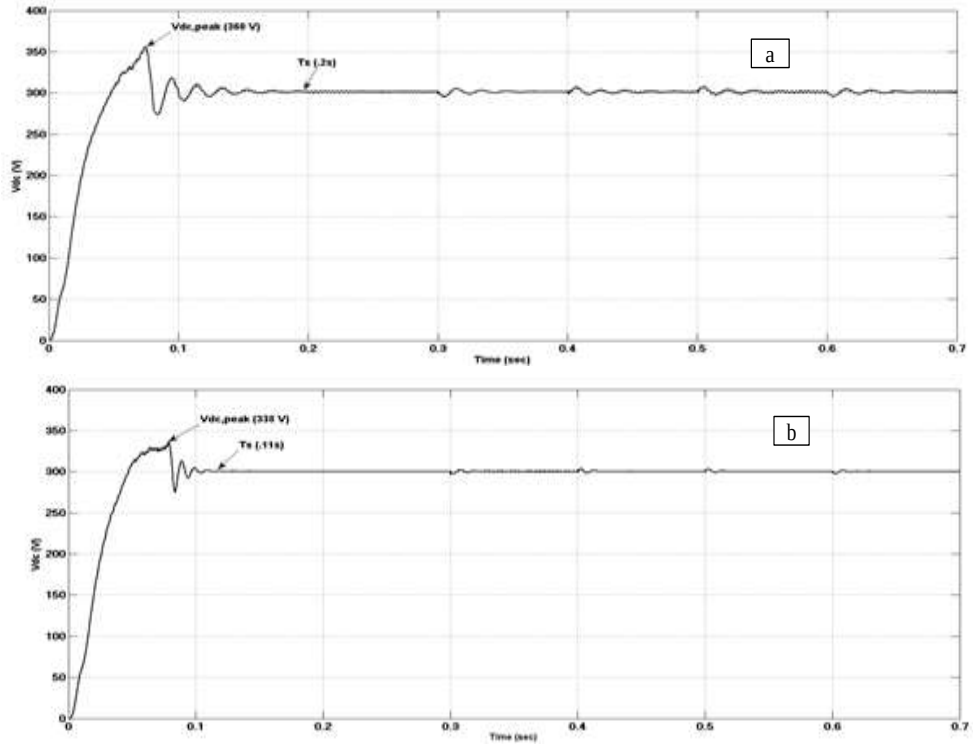


Figure 21. (a) DC bus voltage V_{dc} using PI controller
(b) DC bus voltage V_{dc} using FLC controller

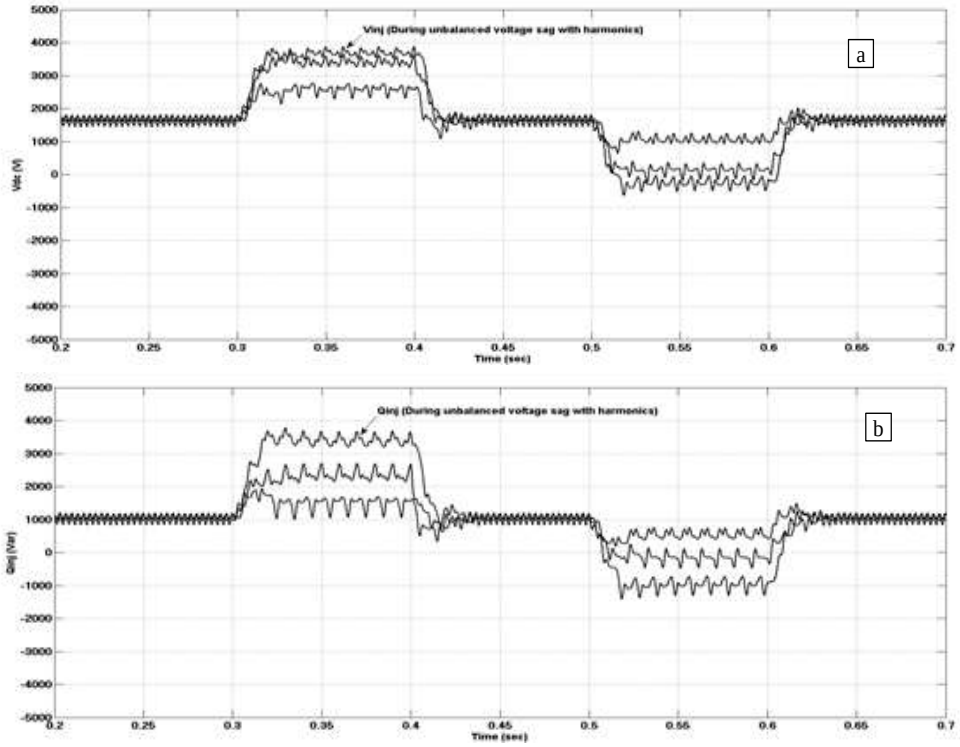


Figure 22. (a) Reactive power injection (Q_{Var}) using PI controller
(b) Reactive power injection (Q_{Var}) using FLC controller

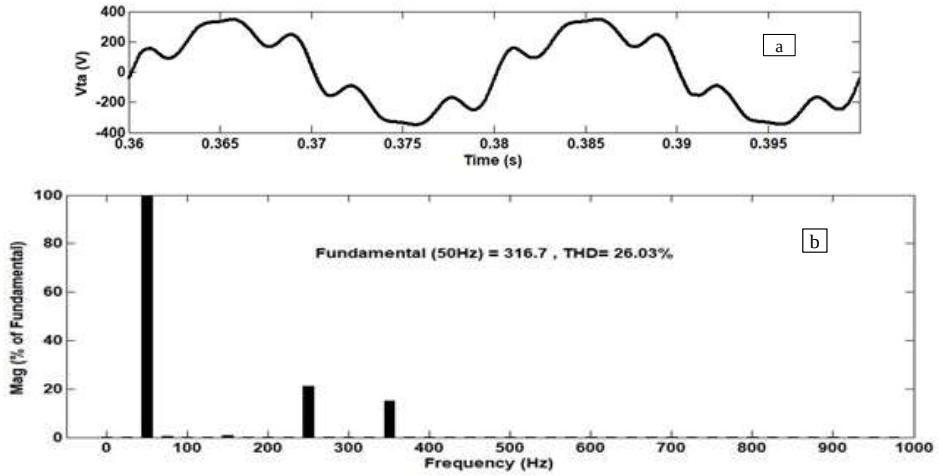


Figure 23. (a) Source terminal voltage (b) Harmonic spectrum

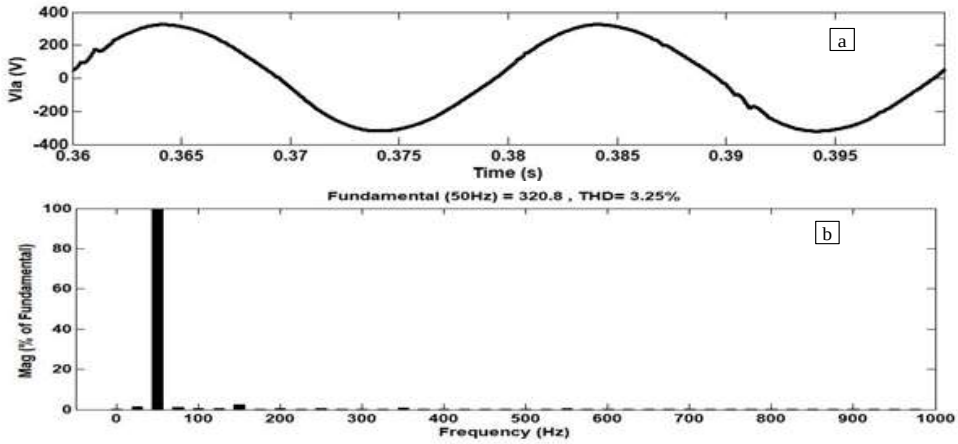


Figure 24. (a) Load voltage (b) Harmonic spectrum

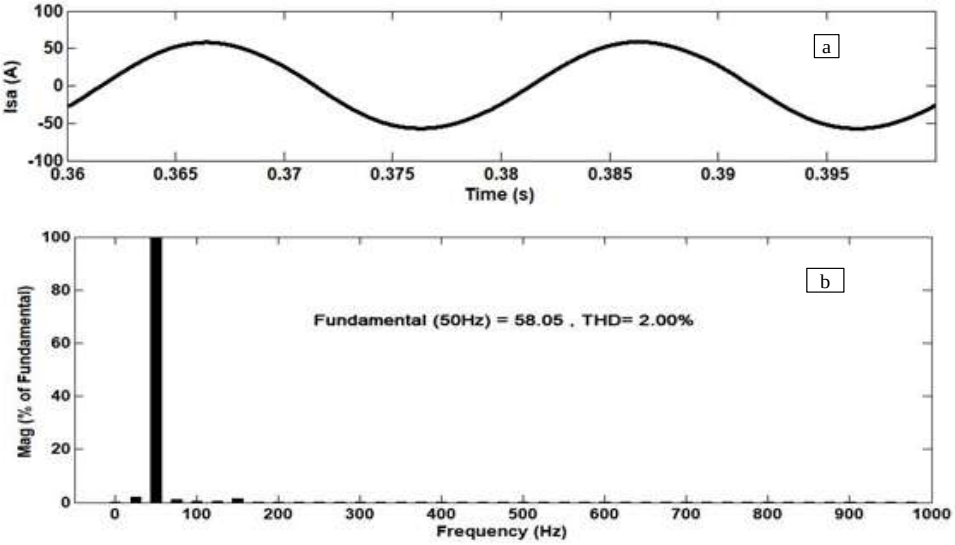


Figure 25. (a) Source current (b) Harmonic spectrum

6. RT-Lab Experimental Results and Discussion

A real time digital simulator is used to validate the proposed control algorithm to control the DVR. The schematic diagram of laboratory set-up is shown in Figure 26. A PC installed with OPAL-RT lab software is used for the performance analysis of DVR in real time. OPAL-RT is a real time simulator with Intel Xeon 3.5 GHz processor, X11SSM-E-F-O Supermicro Server Motherboard and Intel Socket H4 LGA-1155 μTAX working under RT-Lab environment. OPAL-RT can work in real time; it can solve the mathematical equations fast enough to continuously produce output conditions that represent realistic condition in the actual power system. There are 16 analog inputs, 16 analog outputs, 32 digital inputs and 32 digital outputs in OPAL-RT. DVR has two parts, first is control algorithm and second is power circuit components such as three-phase programmable voltage source, three phase critical load, injection transformer, ripple filters and VSI. Both parts of DVR are implemented in OPAL-RT. In industrial applications, the digital controller in OPAL-RT will remain same and power circuit components will be replaced by actual power source, three phase critical load, VSI, ripple filter and injection transformer. All the signals are normalized to 5 V scale because the maximum limit for the I/O signals in OPAL-RT limited to +/- 16 V. The sampling time of OPAL-RT is 10 μS.

The proposed control algorithm for DVR is tested in real time for various types of power quality problems as:

1. During balanced voltage sag
2. During unbalanced voltage sag
3. During balanced voltage swell
4. During unbalanced voltage swell
5. During voltage harmonic distortion

The performance of DVR during balanced sag is shown in Figure 26. It is mandatory to note that the system parameters similar to simulation studies are taken for the experimental validation. Initially, the system is in steady state, suddenly a balanced voltage sag of 15% of magnitude for 3 cycles of AC mains is introduced at PCC. The source voltage, DVR injected voltage, desired load voltage and DC link voltage are taken on Digital Storage Oscilloscope as depicted in Figure 26(a-c). It is clear that proposed control algorithm is sufficient to mitigate the voltage sag and maintains the load voltage at desired value. DC link voltage is fixed at its desired value as shown in Figure 26(c).

The performance of DVR during unbalanced sag is shown in Figure 27. Unbalanced voltage sag of 15% of magnitude in two phases for 3 cycles of AC mains is introduced at PCC. The source voltage, DVR injected voltage, desired load voltage and DC link voltage are depicted in Figure 27(a-c). It is clear that proposed control algorithm is sufficient to mitigate the unbalanced voltage sag and maintains the load voltage at desired value. DC link voltage is fix at its desired value as shown in Figure 27(c).

The performance of DVR during balanced voltage swell is shown in Figure 28. A balanced voltage swell of 15% of magnitude for 3 cycles of AC mains is introduced at PCC. The source voltage, DVR injected voltage, desired load voltage and DC link voltage are depicted in Figure 28(a-c). It is clear that proposed control algorithm is sufficient to mitigate the balanced voltage swell and maintains the load voltage at desired value. DC link voltage is fix at its desired value as shown in Figure 28(c).

The performance of DVR during unbalanced voltage swell is shown in Figure 29. An unbalanced voltage swell of 15% of magnitude in two phases for 3 cycles of AC mains is introduced at PCC. The source voltage, DVR injected voltage, desired load voltage and DC link voltage are depicted in Figure 29(a-c). It is clear that proposed control algorithm is sufficient to mitigate the balanced voltage swell and maintains the load voltage at desired value. DC link voltage is fixed at its desired value as shown in Figure 29(c).

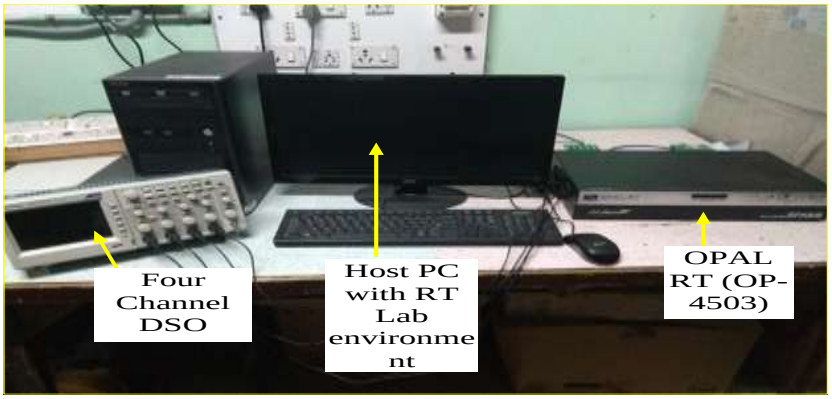
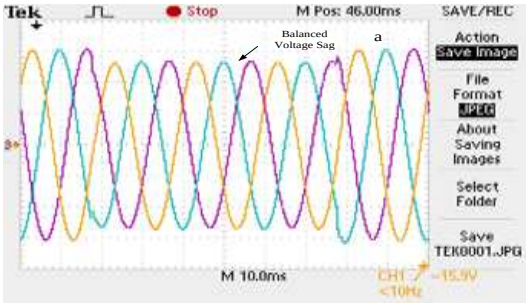
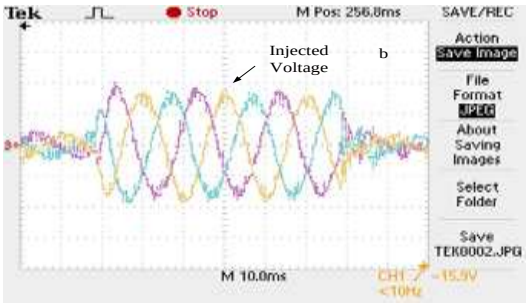


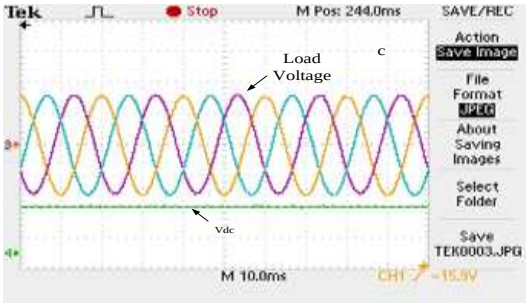
Figure 26. Laboratory set-up



(a)



(b)

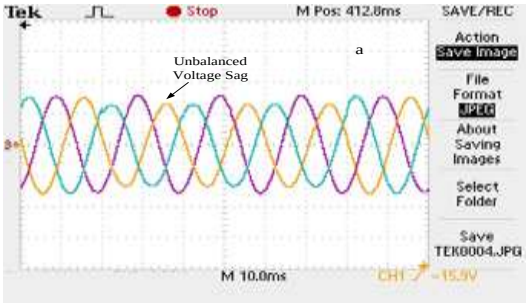


(c)

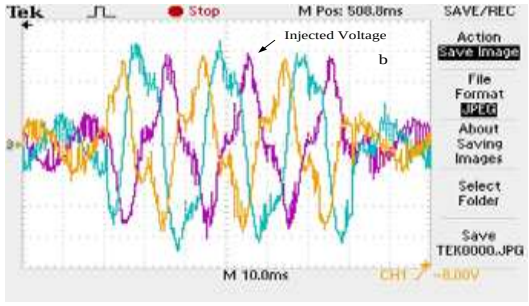
Figure 27. (a) Source voltage during Balanced Voltage sag
(b) Injected Voltage (c) Load Voltage and DC link Voltage

The performance of DVR during voltage harmonic distortion is shown in Figure 30. 5th (20%) and 7th (14%) harmonics distortion is inserted in the supply voltage by the programmable voltage source in all the three phases. DVR injects proper amount of compensation voltage to regulate the load voltage and make it sinusoidal in nature. The source voltage, DVR injected voltage, desired load voltage and DC link voltage are depicted in Figure 30(a-c). The total harmonics distortion of the load voltage well <5%, the limit imposed by IEEE-519 standard.

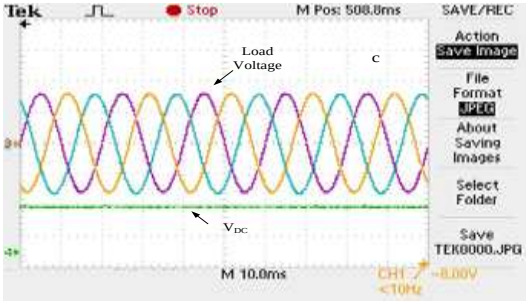
The experimental studies prove that proposed control algorithm is sufficient to tackle major voltage-related power quality issues.



(a)

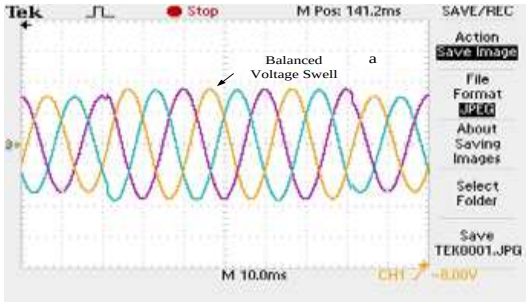


(b)

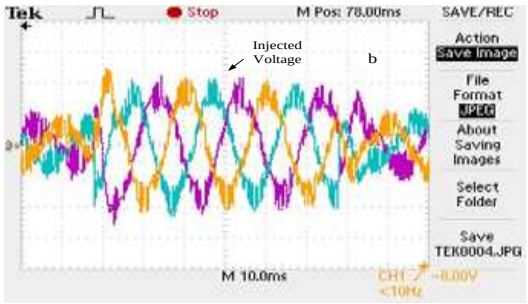


(c)

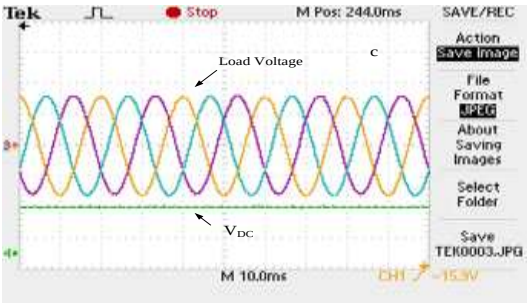
Figure 28. (a) Source voltage during Unbalanced Voltage sag (b) Injected Voltage (c) Load Voltage and DC link Voltage



(a)

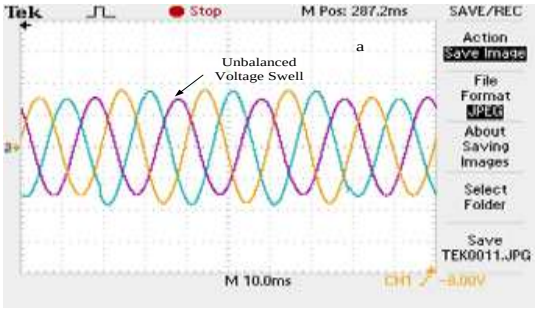


(b)

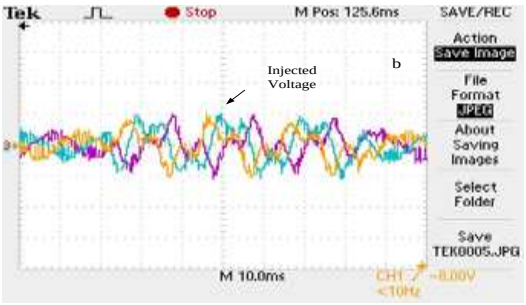


(c)

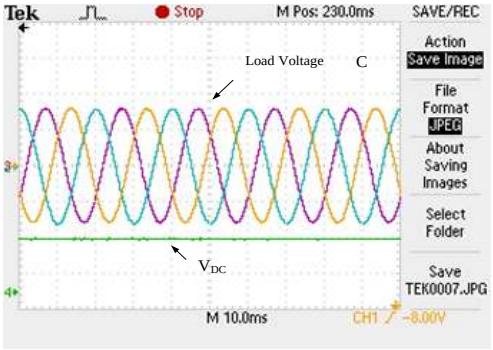
Figure 29. (a) Source voltage during Balanced Voltage swell
(b) Injected Voltage (c) Load Voltage and DC link Voltage



(a)

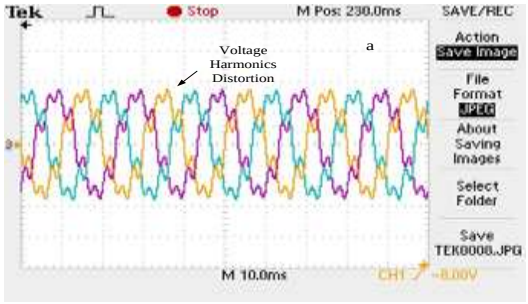


(b)

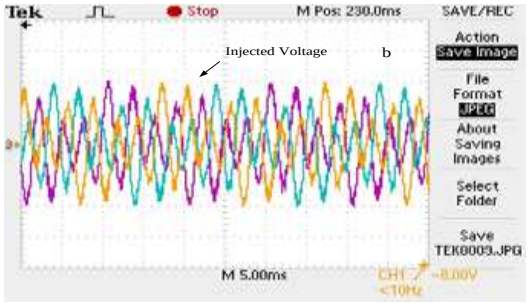


(c)

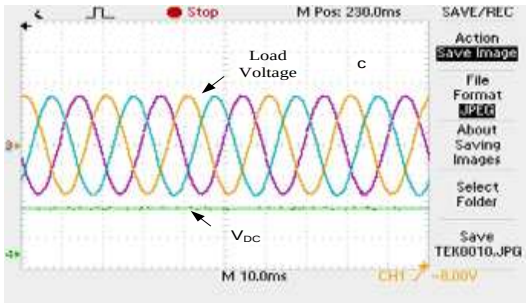
Figure 30. (a) Source voltage during Unbalanced Voltage swell (b) Injected Voltage (c) Load Voltage and DC link Voltage



(a)



(b)



(c)

Figure 31. (a) Source voltage during Voltage harmonics distortion (b) Injected Voltage (c) Load Voltage and DC link Voltage

6. Conclusion

In this paper, reduced-rule based Sugino-type fuzzy logic controller based on SRF theory is implemented for efficient control of DVR to address various source-side power quality problems. The proposed reduced-rule base fuzzy logic controller is capable to mitigating most types of power quality problems at source side i.e. balanced as well as unbalanced voltage sag/swell, voltage harmonic distortion and balanced as well as unbalanced voltage sag/swell with harmonic distortion. The advantage of proposed controller is that in future we can easily increase the number of rules for considering other severe types of power quality problems at the source side. This makes the controller more flexible, less complex and robust in nature. The fuzzy logic controller based DVR reduces overshoot in DC bus voltage, damps out oscillations in DC bus voltage quickly and reduces the cost of DVR converter by way of reducing the injection of reactive power compared to PI controller based DVR. The reduced rule fuzzy based DVR requires least control effort as compared to conventional PI based DVR. The simulation results are experimentally verified showing the excellent performance of DVR under various types of power quality problems at source side.

7. References

[1]. IEEE 100, The Authoritative Dictionary of IEEE Standard Terms, seventh edition, 2000, p. 234.

[2]. M.H.J. Bollen, "Understanding power quality problems- voltage sags and interruptions," in IEEE Press, 2000.

[3]. R.C. Dugan, M.F. Granaghan, S. Santoso and H.W.Beaty, "Electrical Power Systems Quality," 2nd Edition, McGraw Hill, 2004.

[4]. IEEE Std. 1159-1995. Recommended Practice for Monitoring Electric Power Quality.

[5]. J. Rana, C. K. Vasoya, M. H. Pandya and P. M. Saradva, "Application of Unit Template Algorithm for voltage sag mitigation in distribution line using D-STATCOM," *2016 International Conference on Energy Efficient Technologies for Sustainability (ICEETS)*, Nagercoil, 2016, pp. 756-761.

[6]. S. R. Arya, R. Niwas, K. Kant Bhalla, B. Singh, A. Chandra and K. Al-Haddad, "Power Quality Improvement in Isolated Distributed Power Generating System Using DSTATCOM," in *IEEE Transactions on Industry Applications*, vol. 51, no. 6, pp. 4766-4774, Nov.-Dec. 2015.

[7]. Kumar, A. H. Bhat and S. P. Singh, "Performance evaluation of fuzzy logic controlled voltage source inverter based unified power quality conditioner for mitigation of voltage and current harmonics," *2016 International Conference on Advances in Computing, Communications and Informatics (ICACCI)*, Jaipur, 2016, pp. 1799-1804.

[8]. Ghosh, A. K. Jindal and A. Joshi, "Design of a capacitor-supported dynamic voltage restorer (DVR) for unbalanced and distorted loads," in *IEEE Transactions on Power Delivery*, vol. 19, no. 1, pp. 405-413, Jan. 2004.

[9]. P. Kanjiya, B. Singh, A. Chandra and K. Al-Haddad, "'SRF Theory Revisited" to Control Self-Supported Dynamic Voltage Restorer (DVR) for Unbalanced and Nonlinear Loads," in *IEEE Transactions on Industry Applications*, vol. 49, no. 5, pp. 2330-2340, Sept.-Oct. 2013.

[10]. J. G. Nielsen and F. Blaabjerg, "A detailed comparison of system topologies for dynamic voltage restorers," in *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1272-1280, Sept.-Oct. 2005.

[11]. P. Jayaprakash, B. Singh, D. P. Kothari, A. Chandra and K. Al-Haddad, "Control of Reduced-Rating Dynamic Voltage Restorer With a Battery Energy Storage System," in *IEEE Transactions on Industry Applications*, vol. 50, no. 2, pp. 1295-1303, March-April 2014.

[12]. Singh, P. Jayaprakash and D.P. Kothari, " Adaline Based Control of Capacitor Supported DVR for Distribution Systems," *Journal of Power Electronics*, Vol. 9, No. 3, May 2009.

[13]. R. S. Bajpai and R. Gupta, "Series compensation to mitigate harmonics and voltage sags/swells in distributed generation based on symmetrical components estimation," *2011 IEEE International Symposium on Industrial Electronics*, Gdansk, 2011, pp. 1639-1644

[14]. R. Omar and N. A. Rahim, "Implementation and control of a dynamic voltage restorer using Space Vector Pulse Width Modulation (SVPWM) for voltage sag mitigation," *2009 International Conference for Technical Postgraduates (TECHPOS)*, Kuala Lumpur, 2009, pp. 1-6.

[15]. Kumar and M. K. Mishra, "Predictive Voltage Control of Transformerless Dynamic Voltage Restorer," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 2693-2697, May 2015.

[16]. M. Mahalakshmi, S. Latha and S. Ranjithpandi, "Sliding mode control for PMSG Based Dynamic Voltage Restorer," *2013 International Conference on Energy Efficient Technologies for Sustainability*, Nagercoil, 2013, pp. 1320-1323.

[17]. M. Vilathgamuwa, A. A. D. Ranjith Perera, S. S. Choi and K. J. Tseng, "Control of energy optimized dynamic voltage restorer," *Industrial Electronics Society, 1999. IECON '99 Proceedings. The 25th Annual Conference of the IEEE*, San Jose, CA, 1999, pp. 873-878 vol.2.

[18]. Sang-Joon Lee, Hyosung Kim, Seung-Ki Sul and F. Blaabjerg, "A novel control algorithm for static series compensators by use of PQR instantaneous power theory," in *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 814-827, May 2004.

[19]. Qiang Lu, Feng Liu, Shengwei Mei and M. Goto, "Nonlinear disturbance attenuation control for STATCOM," *2001 IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No.01CH37194)*, Columbus, OH, 2001, pp. 1323-1328 vol.3.

[20]. S. Solat, M. Moallem and M. A. Latify, "A supervisory hierarchical fuzzy controller for dynamic voltage restorer (DVR)," *2015 23rd Iranian Conference on Electrical Engineering*, Tehran, 2015, pp. 1694-1699.

[21]. S. P. Singh, A. H. Bhat and A. Kumar, "Fuzzy logic based dynamic voltage restorer for addressing various power quality problems," *2016 IEEE 7th Power India International Conference (PIICON)*, Bikaner, 2016, pp. 1-5.

[22]. Hamoud, M. L. Doumbia, A. Chériti and H. Teiar, "Power factor improvement using adaptive fuzzy logic control based D-STATCOM," *2017 Twelfth International Conference on Ecological Vehicles and Renewable Energies (EVER)*, Monte Carlo, 2017, pp. 1-6.

[23]. Kumar and M. K. Mishra, "A modified DSTATCOM topology with reduced VSI rating, DC link voltage, and filter size," *2013 International Conference on Clean Electrical Power (ICCEP)*, Alghero, 2013, pp. 325-331

[24]. R. K. Agarwal, I. Hussain and B. Singh, "LMF-Based Control Algorithm for Single Stage Three-Phase Grid Integrated Solar PV System," in *IEEE Transactions on Sustainable Energy*, vol. 7, no. 4, pp. 1379-1387, Oct. 2016.

[25]. N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics: Converters Applications and Design. New York, NY, USA: Wiley, 2003

[26]. R. K. Agarwal, I. Hussain and B. Singh, "Three-phase single-stage grid tied solar PV ECS using PLL-less fast CTF control technique," in IET Power Electron., Vol. 10, Iss. 2, pp. 178–188,2017

[27]. Suresh Mikkili, Anup Kumar Panda, "Types-1 and -2 Fuzzy logic controllers-based shunt active filter Id–Iq control strategy with different Fuzzy membership functions for power quality improvement using RTDS hardware," IET Power Electronics, Vol. 6, Issue 4, pp. 818 – 833, April 2013.

[28]. S. Mohagheghi, G. K. Venayagamoorthy, S. Rajagopalan and R. G. Harley, "Hardware Implementation of a Mamdani Fuzzy Logic Controller for a Static Compensator in a Multimachine Power System," in *IEEE Transactions on Industry Applications*, vol. 45, no. 4, pp. 1535-1544, July-aug. 2009.

[29]. Taeed, Z. Salam and S. Ayob, "FPGA Implementation of a Single-Input Fuzzy Logic Controller for Boost Converter with the Absence of an External Analog-to-Digital Converter," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 1208-1217, Feb. 2012.

Shubhendra Pratap Singh received the BE degree in Electronics and Communication Engineering from Jaipur, India. Received M.Tech degree in Electrical Power and Energy System from National Institute of Technology Srinagar, India. Currently he is pursuing his PhD programme in Electrical Engineering in the department of Electrical Engineering, National Institute of Technology Srinagar, India. His areas of interest are power quality, power electronics and custom power devices.

Abdul Hamid Bhat received the B.Tech degree in Electrical Engineering from National Institute of Technology Srinagar, India. Received M.Tech and Ph.D degrees in Electrical Engineering from Indian Institute of Technology Roorkee, India. Currently he is working as Professor and Head in Department of Electrical Engineering, National Institute of Technology Srinagar. His areas of interest are power quality, power electronics, FACTS, custom power devices, improved power quality converters and electrical drives.

Arfat Firdous received Ph.D in Physics in Department of Physics from National Institute of Technology Srinagar, India. Currently he is working as Sr. Assistant Professor in department of physics, Govt. Degree College Tral, Department of higher education, J & K India.