Neutral Point Potential Control for Three Phase 3-level Neutral Point Clamped Active Front End Converter

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Abstract: The use of power electronic converters influences the generation of harmonics and reactive power flow in power system. Therefore, three-phase multilevel improved power quality AC-DC converters are gaining lot of popularity in power conversion applications. This work deals with critical problem of multilevel structure i.e. neutral point potential (NPP) variation. In this paper, a simplified current controlled scheme is presented to ensure unity power factor operation. Neutral point potential (NPP) of three-phase, 3-level NPC AC-DC converter is controlled by modifying control signal in the controller using NPP regulator. An auxiliary circuit is being presented in this paper as an alternative option for controlling the neutral point potential of the converter. Comparison has been carried out between these control techniques in terms of power quality. A complete mathematical model is presented for better understanding of both techniques used for NPP control. The presented control techniques has been verified through simulation investigations and validated experimentally on the developed laboratory prototype.

Keywords: AC-DC converters, Active Front End Converter, Multilevel Converter, Neutral Point Clamped Converter, Unity Power Factor Controller (UPC).

1. Introduction

AC-DC power converters have been widely used in various applications like front end converters in adjustable speed AC drives, High Voltage DC Transmission, Switch Mode Power Supply, utility interface with non-conventional energy source etc. [1]. Traditionally uncontrolled rectifier or SCRs used for AC-DC conversion suffer from some inherent problems like drawing harmonic currents and reactive component of the current from the source and offering highly nonlinear characteristic. Current harmonics generated by these nonlinear loads further result in voltage distortion which is becoming troublesome for the operation of many sensitive equipment and other consumer loads [2-3].

Therefore, high power factor converters (HPFC) has became the inherent part of AC-DC conversion because of its important features like conversion at unity power factor with higher efficiency, reduced size and well regulated dc output [4-8]. But these high power factor converters using high voltage rating devices are having limitations such as large dv/dt, large voltage stress across switching device, large common mode voltage generation, high switching frequency etc. [9-12]. A new age of converters i.e. multilevel structure is gaining lot of popularity because of its excellent performance in terms of improved power quality, less ripple in regulated dc output voltage, reduced voltage stress across switch, reduced dv/dt and low electromagnetic interference with neighbouring communication lines as compared to its counterpart 2-level HPFCs [13-18].

Diode Clamped Multilevel Converter topology which is most widely used topology in multilevel power conversion [9-11], suffers from the problem of unbalanced voltages across dc link capacitors [19]. The voltage equalization of dc link capacitors is the necessary precondition for stable operation of a diode clamped multilevel converters [20].

Several control techniques based on sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) [21-25] have already been proposed to mitigate this
problem. Another way to control neutral point potential in multilevel converters is the use of additional voltage regulators, separate dc sources or additional circuit to balance the voltage across the capacitors [19, 26]. The problem with the auxiliary circuits used for balancing purpose is the extra cost of the switching devices, inductors, capacitors as well as higher switching losses. Literatures are now available for reducing switching losses in multilevel structures [28, 29].

In this paper, unity power factor controller (UPC) is presented to ensure unity power factor operation of three-phase, 3-level NPC AC-DC converter. A comparative study has been carried out between neutral point potential (NPP) regulator in UPC and an auxiliary circuit for controlling the NPP. The aim of this study is to address adverse effects of NPP regulator in UPC to control NPP in terms of power quality. A simple concept based on ping-pong theory to control NPP, is discussed in this paper as an alternative option for balancing of dc link capacitor voltages on the cost of extra hardware and higher losses. The complete working with mathematical modelling of auxiliary circuit based on ping-pong theory is presented. Experimentation is performed on the prototype developed in the laboratory to validate the effective working of controllers.

2. Neutral Point Clamped Active Front end 3-Level Converter

A three phase neutral-point clamped active front end 3-level converter is shown in Figure 1. There are four power switches (S_{a1}, S_{a2}, S'_{a1} and S'_{a2} for phase ‘a’) in one leg for each phase and each leg is having two clamping diodes (D_{a1} & D_{a1} for phase ‘a’). Active front end rectifier is fed by 3-phase AC source connected through boost inductor (L_s). C_1 and C_2 are the dc link capacitors, midpoint of dc link capacitors and clamping diodes of each leg is connected to the neutral of three phase AC source. Resistance R_1 and R_2 are connected across the dc link capacitors to include loading effect of active front end converter [30].

![Figure 1. Neutral point clamped active front end 3-level converter](image)

The independent power switches (S_{x1}, S_{x2}, S'_{x1} and S'_{x2}, x = a, b, c) are controlled in each leg of the converter. The constraints for four power switches in each leg of the converter are defined so as to avoid the conduction of a power switches of the same leg conducting simultaneously.

\[ S_{xi} + S'_{xi} = 1 \]  
where x = a, b, c and i = 1, 2.

\[ S_{xi} = 1, \text{ if the switch } S_{xi} \text{ is turned on or } S_{xi} = 0, \text{ if the switch } S_{xi} \text{ is turned off.} \]  
The equivalent switching function of the rectifier is given below-
Neutral Point Potential Control for Three Phase 3-level Neutral Point

\[
T_{Sx} = \begin{cases} 
1 & \text{if } S_{x1} = S_{x2} = 1 \\
0 & \text{if } S'_{x1} = S_{x2} = 1 \\
-1 & \text{if } S'_{x1} = S'_{x2} = 1 
\end{cases} \tag{2}
\]

Therefore, three valid operating modes in leg ‘a’ of the converter are possible and Table 1 shows the valid switching states of the power switches of three legs and the corresponding voltages on the ac side of the rectifier. Though, it has so many advantages over its counterpart conventional 2-level converters, it suffers from serious problem of unbalance voltage of dc link capacitors under unbalanced loading conditions.

<table>
<thead>
<tr>
<th>T</th>
<th>S_{x1}</th>
<th>S_{x2}</th>
<th>S'_{x1}</th>
<th>S'_{x2}</th>
<th>V_{xn}</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>V_{c1} = V_o/2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>- V_{c2} = V_o/2</td>
</tr>
</tbody>
</table>

\(x = a, b, c\).

In the following sections the working of UPC has been explained which includes the explanation regarding the functioning of neutral point potential (NPP) regulator as well as the concept to balance dc link voltage based on ping pong theory using auxiliary circuit.

The voltage equalization of dc link capacitors is the necessary precondition for stable operation of a diode clamped multilevel converters. Therefore, an appropriate control is required to balance the dc link voltage along with power factor control.

3. Unity Power Factor Controller

A simplified current control scheme as shown in Figure. 2 is implemented to ensure unity power factor operation as well as improved power quality operation of the converter and termed as unity power factor controller (UPC). The UPC comprises of a voltage controller, neutral point potential regulator (NPP) and current controller [30].

![Figure 2. Schematic diagram of neutral point clamped active front end 3-level converter control scheme (UPC)](image)

As shown in Figure. 2, a proportional integral voltage controller is used to balance AC side power and DC side power of the rectifier, to obtain the amplitude of the line current command i.e. I_m. The current command can be written as,
\[ I_m = k_p \Delta V_0 + k_i \int \Delta V_0 \]  \hspace{1cm} (3)

where \( \Delta V = V^* - V_0 \) is the DC bus voltage error, \( V^* \) is the reference DC link voltage command and \( V_0 \) is the measured DC link voltage. The unit sinusoidal voltages generated through PLL can be written as-

\[
\begin{align*}
V_{sau(t)} &= \sin(\omega t) \\
V_{sba(t)} &= \sin(\omega t + 2\pi/3) \\
V_{sca(t)} &= \sin(\omega t - 2\pi/3)
\end{align*}
\]  \hspace{1cm} (4)

The line current commands are derived from the multiplication of the output of the voltage controller with the unit sinusoidal voltages and the resultant is then added to the output of the NPP regulator as shown in Figure 2.

\[
\begin{align*}
i_{a}^{*}(t) &= I_m \sin(\omega t) \\
i_{b}^{*}(t) &= I_m \sin(\omega t - 2\pi/3) \\
i_{c}^{*}(t) &= I_m \sin(\omega t + 2\pi/3)
\end{align*}
\]  \hspace{1cm} (5)

![Graph showing line current commands](image)

The measured line current and respective reference line currents are transformed to dq reference frame before feeding to current controller to track the source current commands. Neglecting the high-frequency switching terms, we can write source voltage of phase ‘a’.

\[ V_{sa} = L_{sa} \frac{di_{sa}}{dt} + V_{con_a} \]  \hspace{1cm} (6)

where \( V_{con_a} \) is the modulated control signal of PWM converter derived from the proposed closed loop control of the system. The carrier-based sinusoidal PWM scheme is employed for generating proper switching signals as shown in Figure 3.
Figure 3. (a) Carrier-based PWM scheme for the generation of gating pulses (b) Obtained gating pattern

Based on above control scheme and gating signals, the switching signals of the power switches can be defined as-

\[ T_c = \begin{cases} 
1 & \text{if } v_{cona} > v_{11} \\
0 & \text{if } v_{11} > v_{cona} > v_{22} \\
-1 & \text{if } v_{22} > v_{cona} 
\end{cases} \]  

Hence switching function can be written as-

\[
S_{a1} = \frac{T_c(T_c + 1)}{2} \\
S'_{a1} = 1 - S_{a1} \\
S_{a2} = \frac{T_c(T_c + 1)}{2} \\
S'_{a2} = 1 - S'_{a2}
\]  

Therefore for phase ‘a’, in the positive half of the control signals V_{cona}, the power switch S_{a2} is turned on and the line current is controlled by turning on or off the power switch S_{a1}. In the negative half of V_{cona}, S_{a1} is turned off and turning on or off S_{a2} can control the line current to follow the current command. For equal capacitor voltages (V_{c1} = V_{c2} = V_o/2), three voltage levels (V_o/2, 0, and - V_o/2) are generated on the AC side of the rectifier phase voltage V_{an}.

A. NPP Regulator in UPC

Neutral point potential (NPP) can be controlled using general law for the neutral point current, the dc side quantities are given as under,

(assuming \( C_1 = C_2 \))

\[ i_1 = C \frac{dV_{c1}}{dt} \]  

\[ i_2 = C \frac{dV_{c2}}{dt} \]
Neutral point current is given by
\[ i_0 = -i_1 + i_2 \]  
and
\[ i_0 = -C \frac{d(V_{c1} - V_{c2})}{dt} \]  

The equation yields
\[ V_{c1} - V_{c2} = -\frac{1}{C} \int i_0 dt + \text{cons} \tan t \]  

This signifies that a DC component in the neutral current \( i_0 \), can be utilised to compensate the voltage dc link capacitor voltages of the converter.

**B. Auxiliary Circuit**

As shown in the Figure 4 dc link capacitors \( C_1 \) and \( C_2 \) are connected to an auxiliary capacitor \( C_a \) through four switches. A series resistance \( r \) is connected with auxiliary capacitor \( C_a \) to limit the amplitude of the charging current for practical consideration. Whenever there is voltage difference between \( C_1 \) and \( C_2 \) there will be always charging and discharging current between one of the dc link capacitors (\( C_1 \) or \( C_2 \)) and auxiliary capacitor \( C_a \). To explain the balancing phenomena the whole operation is divided into four cases.

**Case 1: When \( V_{c1} > V_{ca} \)**

In this condition, switch \( S1 \), \( S3 \) are turned on and switch \( S2 \), \( S4 \) are turned off. The charging current \( i_{ca} \) pumps from \( C_1 \) to \( C_a \) through \( S1 \), \( r \) and \( D3 \) as highlighted in Figure 5a.
Case 2: When $V_{c1} < V_{ca}$
When voltage across auxiliary capacitor ($V_{ca}$) is more than dc link capacitor $V_{c1}$, the switching action will remain the same i.e. $S1$, $S3$ are on and charging current $i_{ca}$ comes from $C_{a}$ through $r$, $D1$, $C_{1}$ and $S3$ as highlighted in Figure 5b.

Figure 5b. Current flows from $C_{a}$ to $C_{1}$

Case 3: When $V_{c2} < V_{ca}$
Under this condition, the switch $S1$, $S3$ are turned off and $S2$, $S4$ are now turned on. The charging current $i_{ca}$ comes from $C_{a}$ to $C_{2}$ through $r$, $S2$, $D4$ as highlighted in Figure 5c.

Figure 5c Current flows from $C_{a}$ to $C_{2}$

Case 4: When $V_{c2} > V_{ca}$
In this condition, switching action will again remain the same and the charging current $i_{ca}$ pumps from $C_{2}$ to $C_{a}$ through $D2$, $r$ and $S4$ as highlighted in Figure 5d.

Figure 5d. Current flows from $C_{2}$ to $C_{a}$

The equivalent circuit for the Figure.4 is drawn and shown in the Figure.6. For the analysis purpose the equivalent circuit is drawn for Case 1 and Case 2 and same analysis is applicable for Case 3 and Case 4.
If $C_1$ and $C_a$ are equal then the total capacitance of capacitors in series is equal to $C/2$. The voltage and the charging current in the simple RC circuit will be given below for the time period of $t_0$ to $t_1$.

$$V(t) = V(t_0) - \frac{2}{C} \int_{t_0}^{t_1} i_{c1}(t) \, dt$$  
$$i_{c1}(t) = \frac{V(t_0)}{r} e^{-\frac{2t}{\tau}}$$  

As explained earlier the balancing concept is based on ping pong operation and one ping pong operation is divided into two time steps. Step 1 starts from time $t_0$ and finish at $t_1$ corresponding to Case 1 & 2 of earlier section whereas time period for step 2 is $t_1$-$t_2$ corresponding to Case 3 & 4 of earlier section. Then, the voltages across the $C_1$, $C_2$ and $C_a$ can be expressed as.

$$v_{c1}(t) = \begin{cases} 
    v_{c2}(t_0) - \frac{1}{C} \int_{t_0}^{t_1} i_{ca1}(t) \, dt, & t_0 \leq t \leq t_1 \\
    v_{c1}(t_0), & t_1 \leq t \leq t_2 \\
    v_{c2}(t_1) - \frac{1}{C} \int_{t_1}^{t_2} i_{ca1}(t) \, dt, & t_1 \leq t \leq t_2 
\end{cases}$$  

$$v_{c2}(t) = \begin{cases} 
    v_{c1}(t_0), & t_0 \leq t \leq t_1 \\
    v_{c1}(t_1) + \frac{1}{C} \int_{t_0}^{t_1} i_{ca1}(t) \, dt, & t_0 \leq t \leq t_1 \\
    v_{c1}(t_1) - \frac{1}{C} \int_{t_1}^{t_2} i_{ca1}(t) \, dt, & t_1 \leq t \leq t_2 
\end{cases}$$  

$$v_{ca1}(t) = \begin{cases} 
    v_{c1}(t_0) - \frac{1}{C} \int_{t_0}^{t_1} i_{ca1}(t) \, dt, & t_0 \leq t \leq t_1 \\
    v_{c1}(t_1) - \frac{1}{C} \int_{t_1}^{t_2} i_{ca1}(t) \, dt, & t_1 \leq t \leq t_2 
\end{cases}$$  

Where the balancing current $i_{ca}$ is

$$i_{ca}(t) = \begin{cases} 
    \frac{v_{c1}(t_0) - v_{ca1}(t_0)}{r} e^{-\frac{2t}{\tau}}, & t_0 \leq t \leq t_1 \\
    \frac{v_{c2}(t_1) - v_{ca1}(t_1)}{r} e^{-\frac{2(t-t_1)}{\tau}}, & t_1 \leq t \leq t_2 
\end{cases}$$  

According to (16-19), the voltage difference between $C_1$ & $C_2$ will decrease after a number of ping-pong operations.

Figure 7 shows the control scheme for the auxiliary circuit. This control scheme is generating PWM pulses for auxiliary circuit switches by comparing a signal of constant magnitude with triangular carrier wave such that S2 & S4 are the complimentary of S1 & S3 respectively for carrying out ping-pong operation.
4. Result and Discussion

In this section, simulation results are presented and verified experimentally by developing laboratory prototype of neutral point clamped (NPC) active front end (AFE) 3-level converter.

A. Simulation Results

Simulation results are given for evaluating the performance of the neutral point clamped (NPC) active front end (AFE) 3-level converter using UPC. The simulation is carried out with and without NPP regulator in the UPC under balanced and unbalanced load conditions. The block diagram of simulation model is shown in Figure. 8 and simulation parameters are given in Table 2. The optimized controller parameters are given in Table 3.

Table 2. Simulation Parameters for NPC AFE 3-Level Converter with UPC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Voltage (RMS)</td>
<td>$V_{LL}$</td>
</tr>
<tr>
<td>Boost Inductor</td>
<td>$L_s$</td>
</tr>
<tr>
<td>AC Link Resistance</td>
<td>$R$</td>
</tr>
<tr>
<td>DC Link Voltage</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>DC Link Capacitance</td>
<td>$C_1/C_2$</td>
</tr>
<tr>
<td>Load Resistance</td>
<td>$R_1 \parallel R_1'$</td>
</tr>
<tr>
<td></td>
<td>$R_2 \parallel R_2'$</td>
</tr>
<tr>
<td>Carrier Frequency</td>
<td>$f_c$</td>
</tr>
</tbody>
</table>
Table 3. Selected UPC Parameters for NPC AFE 3-Level Converter

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Controller Parameters</td>
<td></td>
</tr>
<tr>
<td>Proportional Gain ($K_{cp}$)</td>
<td>0.5</td>
</tr>
<tr>
<td>Integral Gain ($K_{ci}$)</td>
<td>10</td>
</tr>
<tr>
<td>Voltage Controller Parameters</td>
<td></td>
</tr>
<tr>
<td>Proportional Gain ($K_{vp}$)</td>
<td>2</td>
</tr>
<tr>
<td>Integral Gain ($K_{vi}$)</td>
<td>25</td>
</tr>
<tr>
<td>NPP Regulator Parameters</td>
<td></td>
</tr>
<tr>
<td>Proportional Gain ($K_{np}$)</td>
<td>2</td>
</tr>
</tbody>
</table>

A.1 Performance of NPC AFE with UPC

Phase voltage of phase ‘a’, line current of phase ‘a’, dc link capacitor voltages ($V_{c1}$ and $V_{c2}$) and load current ($i_0$) under steady state condition is shown in Figure. 9. This shows the stable operation of neutral point clamped active front end 3-level converter with unity power factor controller under steady state condition, which is essentially required for medium voltage, high power applications.

![Figure 9. Phase voltage ($V_{sa}$), Line current ($i_{sa}$), dc link capacitor voltages ($V_{c1}$ and $V_{c2}$) and load current ($i_0$) of NPC AFE 3-level converter under steady state condition](image)

The dynamic performance of NPC AFE AC-DC converter is also evaluated with sudden load change as shown in Figure. 10 & Figure. 11. It is observed that the dc link capacitor voltages ($V_{c1}$ and $V_{c2}$) settled down to its desired value within 10 cycles, the supply
A.2. Neutral Point Potential (NPP) Control Using NPP Regulator

The neutral point potential is basically difference between two dc link capacitor voltages. Ideally NPP should be zero i.e. balanced dc link capacitor voltages under transient and steady state conditions. In this study, simulation is carried out with and without NPP regulator in UPC under balanced and unbalanced load condition. The level of unbalance is measured by a factor defined as depth of unbalance $\sigma$ as [27]
\[ \sigma = \frac{R_1 - R_2}{R_1 + R_2} \times 100 \]  

(20)

Where \( R_1 \) load resistance is across dc link capacitor \( C_1 \) and \( R_2 \) is load resistance across dc link capacitor \( C_2 \).

The study is carried out for different depth of unbalance (\( \sigma \)) to observe its effect on the performance of NPP regulator in UPC. The system parameters for the simulation are same given in Table 2. The details of loading parameters are given in Table 4.

<table>
<thead>
<tr>
<th>Table 4. Load Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistance (( R_1 )) (( \Omega ))</td>
</tr>
<tr>
<td>---------------------------</td>
</tr>
<tr>
<td>15</td>
</tr>
<tr>
<td>15</td>
</tr>
<tr>
<td>15</td>
</tr>
</tbody>
</table>

Figure 12 shows the NPP variation with and without NPP regulator. It clearly shows that there are variations in average of NPP under balanced load (\( \sigma = 0\% \)). Even though the variation is not large, but it is significant for high voltage and high power applications. When NPP regulator is included in the UPC, the NPP variations got suppressed and NPP become almost zero as shown in the Figure 12. Figure 13 and Figure 14 shows the variations of NPP with and without NPP regulator in UPC for \( \sigma = 20\% \) and \( \sigma = 33.33\% \) respectively. These Figure shows that the variations of NPP increases with depth of unbalance. The NPP regulator in UPC is capable to control the NPP variations as shown in Figure 13 and Figure 14.

Figure 15 shows the dc link capacitor voltages (\( V_{c1} \) & \( V_{c2} \)) before and after the NPP regulator included in the UPC. It also confirms the balancing of dc link capacitor voltages using NPP regulator in UPC.

Table 5 shows that, the NPP regulator in UPC removes the 2\(^{nd}\) harmonic from supply line current whereas the dc off-set appears in the supply line current as depth of unbalance increase. The undesirable dc off-set in supply current will saturate the transformer on the utility side and must be removed from the supply current. Therefore, the NPP regulator in the UPC controls the variations in NPP under balanced load whereas for different depth of unbalance the NPP regulator able to control NPP variations at the cost of dc off-set in supply line current.
Figure 13. NPP before and after NPP regulator is included in UPC at $t = 6$ sec for $\sigma = 20\%$

Figure 14. NPP before and after NPP regulator is included in UPC at $t = 6$ sec for $\sigma = 33.33\%$

Figure 15. DC link capacitor voltages ($V_{c1}$ & $V_{c2}$) before and after NPP regulator is included in UPC at $t = 6$ sec for $\sigma = 33.33\%$
Table 5. Variation of DC offset & 2\textsuperscript{nd} Harmonic with depth of unbalance (\(\sigma\)) in Supply Line Current of Phase a (\(i_{sa}\)) with and without NPP Regulator in UPC

<table>
<thead>
<tr>
<th>Depth of Unbalance ((\sigma))</th>
<th>DC Off-set and 2\textsuperscript{nd} Harmonic in Supply Line Current of Phase a ((i_{sa}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without NPP Regulator</td>
<td>With NPP Regulator (%)</td>
</tr>
<tr>
<td>DC Off-set (%)</td>
<td>2\textsuperscript{nd} Harmonic (%)</td>
</tr>
<tr>
<td>DC Off-set (%)</td>
<td>2\textsuperscript{nd} Harmonic (%)</td>
</tr>
<tr>
<td>0%</td>
<td>0 0</td>
</tr>
<tr>
<td>20%</td>
<td>0 10 15%</td>
</tr>
<tr>
<td>33.33%</td>
<td>0 17 25%</td>
</tr>
</tbody>
</table>

A.3. Neutral Point Potential (NPP) Control Using Auxiliary Circuit

A simulation has been carried out for AC-DC multilevel converter with an auxiliary circuit for \(\sigma = 33.33\%\). As shown in Figure 16 the average NPP is become almost zero when auxiliary circuit is included at \(t = 6\) sec. Figure 17 shows the voltage across the dc link capacitors (\(V_{c1} \& V_{c2}\)) before and after the auxiliary circuit is included in system. The simulation confirms that the adopted voltage balancing scheme using auxiliary circuit is maintaining almost equal voltage across the dc link capacitors. Table 6 also shows that the auxiliary circuit balances dc link voltage without dc offset in the input line current for different depth of unbalance load.

Figure 16. Average NPP when auxiliary circuit is included at \(t = 6\) sec for \(\sigma = 33.33\%\)

Figure 17 DC link voltages (\(V_{c1} \& V_{c2}\)) when auxiliary circuit is included at \(t = 6\) sec for \(\sigma = 33.33\%\)
Table 6. Variation of DC offset & 2nd Harmonic with depth of unbalance (σ) in Supply Line Current of Phase a (i\textsubscript{sa}) with Auxiliary Circuit

<table>
<thead>
<tr>
<th>Depth of Unbalance (σ)</th>
<th>DC Off-set and 2nd Harmonic in Supply Line Current of Phase a (i\textsubscript{sa}) with Auxiliary Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DC Off-set (%)</td>
</tr>
<tr>
<td>0%</td>
<td>0</td>
</tr>
<tr>
<td>20%</td>
<td>0</td>
</tr>
<tr>
<td>33.33%</td>
<td>0</td>
</tr>
</tbody>
</table>

B. Experimental Results

The performance of NPC AFE 3-level converter is verified experimentally on developed low power prototype in laboratory. The experimental parameters for NPC AFE 3-level converter are given in Table 7. The prototype of AC-DC converter includes twelve STGW30N120KD, 1200 volts, 30 amps IGBTs and six fast recovery diodes (16FM120) with two dc link capacitors of 2200mF, 600 V each at input side. The control algorithm is implemented through dSPACE real time interface DS1103. The DS1103 real time hardware implementation board is based upon Texas Instruments TMS320F240, 16 bit fixed point digital signal processor, 250 MHz CPU, 20 MHz clock frequency.

Table 7. Experimental Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Voltage (RMS)</td>
<td>V\textsubscript{LL}</td>
<td>50 V</td>
</tr>
<tr>
<td>Source Inductor</td>
<td>L\textsubscript{s}</td>
<td>7.73mH</td>
</tr>
<tr>
<td>AC Link Resistance</td>
<td>R</td>
<td>0.4 Ω</td>
</tr>
<tr>
<td>DC Link Voltage</td>
<td>V\textsubscript{dc}</td>
<td>80 V</td>
</tr>
<tr>
<td>DC Link Capacitors</td>
<td>C\textsubscript{1} and C\textsubscript{2}</td>
<td>2200 μF</td>
</tr>
<tr>
<td>Load Parameters</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load Resistance</td>
<td>(R\textsubscript{1} and R\textsubscript{2})</td>
<td>15 Ω</td>
</tr>
<tr>
<td>Carrier Frequency</td>
<td>f\textsubscript{c}</td>
<td>2050 Hz</td>
</tr>
</tbody>
</table>

B.1. Performance of NPC AFE with UPC

The line voltage (V\textsubscript{ab}) at supply end, supply phase voltage (V\textsubscript{sa}) and line current (i\textsubscript{sa}) are shown in Figure. 18, which clearly shows unity power factor operation of the converter. The harmonic profile of the line voltage (V\textsubscript{ab}) at supply end and line current (i\textsubscript{sa}) are shown in Figure. 19 (a) and Figure. 19 (b) respectively. The line current (i\textsubscript{sa}) drawn by NPC AFE 3-level converter is having only 2.4% of THD, which is well below the limit imposed by standard IEEE 519.
The performance of NPC AFE 3-level converter under steady state condition has been verified experimentally. The phase voltage ($V_{an}$) at supply end is shown in Figure. 20 under steady state condition which confirms one of the important features of multilevel converter having half of the dc link voltage subjected across the devices. The voltage across the dc link capacitors ($V_{c1}$ and $V_{c2}$) are shown in Figure. 21 under steady state condition. This shows stable operation of converter under steady state condition.
Figure 20. Phase voltage ($V_{an}$) at supply end of NPC AFE 3-level converter under steady state condition

X - axis: Time –10ms/div, Y - axis: $V_{an}$ - 20 V/div

Figure 21. DC link capacitor voltages ($V_{c1}$ and $V_{c2}$) of NPC AFE 3-level converter under steady state condition

X axis: Time- 10ms/div, Y axis: $V_{c1}$ and $V_{c2}$ - 20 V/div

The transient response of the converter is evaluated with sudden change in load. The dc link voltages ($V_{c1}$ and $V_{c2}$) and line current of phase ‘a’ ($i_{sa}$) has been observed when load is suddenly increased as shown in Figure.22. It can be clearly observed that the dc link voltages ($V_{c1}$ and $V_{c2}$) decreased when load is suddenly increased thereafter few cycles the dc link voltages recover to its desired voltage. The behaviour of the converter is also observed when load is reduced. The
dc link voltages suddenly increased and after few cycles it gets back to its desired value, shown in Figure 23. The response of the NPC AFE 3-level converter during transient found satisfactory with UPC, and confirmed that UPC is effectively able to regulate dc link voltage quickly at desired value during transient condition.

Figure 22. DC link capacitor voltages ($V_{c1}$ and $V_{c2}$) and line current ($i_{sa}$) of NPC AFE 3-level converter when load is increased

X - axis: Time – 1s/div, Y - axis: $V_{c1}$ and $V_{c2}$ - 20 V/div, $i_{sa}$ – 4 A/div

Figure 23 DC link capacitor voltages ($V_{c1}$ and $V_{c2}$) and line current ($i_{sa}$) of NPC AFE 3-level converter when load is decreased

X - axis: Time – 1s/div, Y - axis: $V_{c1}$ and $V_{c2}$ - 20 V/div, $i_{sa}$ – 4 A/div
B.2 Neutral Point Potential (NPP) Control with NPP Regulator in UPC

It is experimentally verified that multilevel structures have inherent problem of NPP variation. Figure 24 shows variation of NPP before and after the NPP regulator included in \( t = 3 \) sec for \( \sigma = 33.33\% \), which verifies the effective working of NPP regulator in UPC.

![Figure 24. NPP variation before and after NPP regulator included in UPC at \( t = 3 \) sec for \( \sigma = 33.33\% \) (Control Desk Layout)](image)

B.3 Neutral Point Potential (NPP) Control with Auxiliary Circuit

The function of auxiliary circuit has also been verified experimentally. Figure 25 shows the dc link capacitor voltages (\( V_{c1} \) & \( V_{c2} \)) before and after auxiliary circuit included in the system for \( \sigma = 33.33\% \). As shown in the Figure 25 the dc link capacitators voltages are not completely balanced because of series resistance \( r \) is connected with auxiliary capacitor \( C_a \) to limit the amplitude of the charging current for practical consideration. The presented result confirms the working of auxiliary circuit adopted to balance the dc link capacitors voltage.

![Figure 25. DC link capacitor voltages (\( V_{c1} \) and \( V_{c2} \)) before and after auxiliary circuit included in the system for \( \sigma = 33.33\% \)](image)
X-axis: Time – 1s/div, Y-axis: V_c1 and V_c2 - 20 V/div

4. Conclusion

The unity power factor controller (UPC) is presented to control NPC AFE 3-level converter for improved power quality at input and load side. The performance of three-phase NPC AFE 3-level converter has been evaluated with unity power factor controller. Simulation results are presented to study the performance of the system during transients as well as in steady state. It is observed that 3-level converter is operating at almost unity power factor with supply current THD within the limits imposed by IEEE519 standard. Simulated results also show that NPP regulator in conjunction with UPC is able to balance the capacitor voltages under balanced and unbalanced load with the addition of dc off-set in supply line current. The simulation results with an auxiliary circuit to balance the dc link capacitor voltages show effective balancing of dc link capacitor voltages without any adverse effects in terms of power quality. The features of UPC with NPP regulator and auxiliary circuit, observed in simulation study are also validated through experimentation performed on the low power prototype developed in laboratory using dSPACE DS 1103. Further, it can be concluded that the UPC with NPP regulator is suitable for drives application where depth of unbalance is not much whereas an auxiliary circuit is effective for active power filter where depth of unbalance is high.

5. References

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