Neutral point current is given by

$$i_0 = -i_1 + i_2 \tag{11}$$

$$i_0 = -C\frac{d(V_{c1} - V_{c2})}{dt} \tag{12}$$

The equation yields

$$V_{c1} - V_{c2} = -\frac{1}{C}\int i_0 dt + cons\tan t \tag{13}$$

This signifies that a DC component in the neutral current i_0, can be utilised to compensate the voltage dc link capacitor voltages of the converter.

B. Auxiliary Circuit

As shown in the Figure.4 dc link capacitors C_1 and C_2 are connected to an auxiliary capacitor C_a through four switches. A series resistance r is connected with auxiliary capacitor C_a to limit the amplitude of the charging current for practical consideration. Whenever there is voltage difference between C_1 and C_2 there will be always charging and discharging current between one of the dc link capacitors (C_1 or C_2) and auxiliary capacitor C_a. To explain the balancing phenomena the whole operation is divided in to four cases.

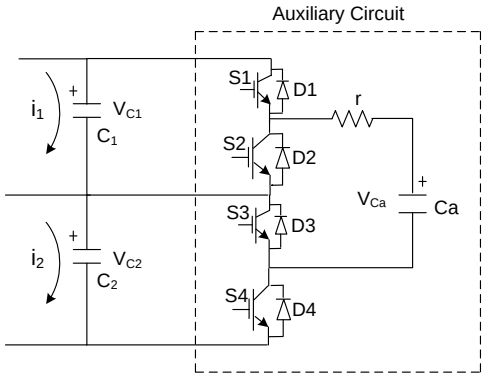


Figure.4 Auxiliary circuit for dc link capacitor voltage balancing

Case 1: When $V_{c1} > V_{ca}$

In this condition, switch S1, S3 are turned on and switch S2, S4 are turned off. The charging current i_{ca} pumps from C_1 to C_a through S1, r and D3 as highlighted in Figure. 5a.

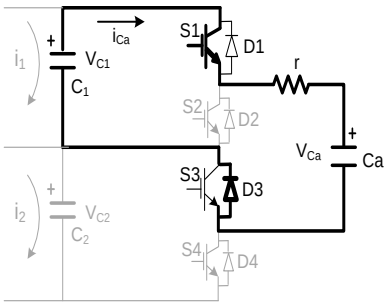


Figure 5a. Current flows from C_1 to C_a

Case 2: When $V_{c1} < V_{ca}$

When voltage across auxiliary capacitor (V_{ca}) is more than dc link capacitor V_{c1}, the switching action will remain the same i.e. S1, S3 are on and charging current i_{ca} comes from C_a through r, D1, C_1 and S3 as highlighted in Figure 5b.

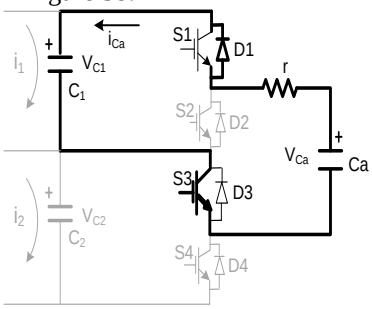


Figure 5b. Current flows from C_a to C_1

Case 3: When $V_{c2} < V_{ca}$

Under this condition, the switch S1, S3 are turned off and S2, S4 are now turned on. The charging current i_{ca} comes from C_a to C_2 through r, S2, D4 as highlighted in Figure 5c.

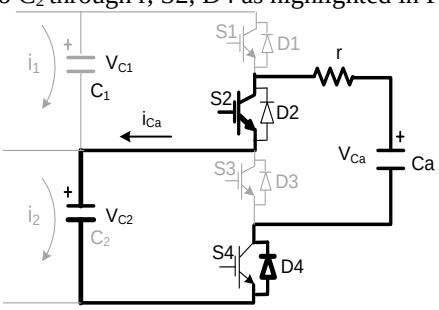


Figure. 5c Current flows from C_a to C_2

Case 4: When $V_{c2} > V_{ca}$

In this condition, switching action will again remain the same and the charging current i_{ca} pumps from C_2 to C_a through D2, r and S4 as highlighted in Figure. 5d.

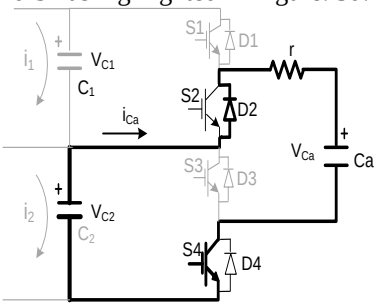


Figure 5d. Current flows from C_2 to C_a

The equivalent circuit for the Figure.4 is drawn and shown in the Figure.6. For the analysis purpose the equivalent circuit is drawn for *Case 1* and *Case 2* and same analysis is applicable for *Case 3* and *Case 4.*

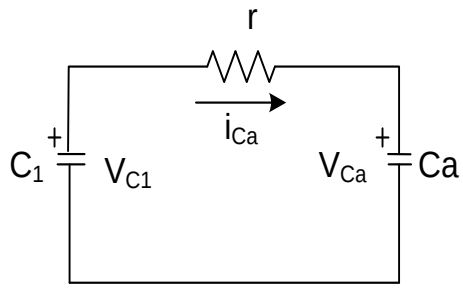


Figure 6. Equivalent circuit

If C_1 and C_a are equal then the total capacitance of capacitors in series is equal to C/2. The voltage and the charging current in the simple RC circuit will be given below for the time period of t_0 to t_1.

$$V(t) = V(t_0) - \frac{2}{C}\int_{t_0}^{t_1} i_{c1}(t)dt \tag{14}$$

$$i_{c1}(t) = \frac{V(t_a)}{r} e^{-\frac{2t}{rc}} \tag{15}$$

As explained earlier the balancing concept is based on ping pong operation and one ping pong operation is divided in to two time steps. Step 1 starts from time t_0 and finish at t_1 corresponding to *Case 1 & 2* of earlier section whereas time period for step 2 is t_1-t_2 corresponding to *Case 3 & 4* of earlier section. Then, the voltages across the C_1, C_2 and C_a can be expressed as,

$$v_{c1}(t) = \begin{cases} v_{c1}(t_0) - \frac{1}{c}\int_{t_0}^{t_1} i_{ca1}(t)dt, & t_0 \le t \le t_1 \\ v_{c1}(t_0), & t_1 \le t \le t_2 \end{cases} \tag{16}$$

$$v_{c2}(t) = \begin{cases} v_{c2}(t_0), & t_0 \le t \le t_1 \\ v_{c2}(t_1) - \frac{1}{c}\int_{t_1}^{t_2} i_{ca1}(t)dt, & t_1 \le t \le t_2 \end{cases} \tag{17}$$

$$v_{ca1}(t) = \begin{cases} v_{c1}(t_0) + \frac{1}{c}\int_{t_0}^{t_1} i_{ca1}(t)dt, & t_0 \le t \le t_1 \\ v_{c1}(t_1) - \frac{1}{c}\int_{t_1}^{t_2} i_{ca1}(t)dt, & t_1 \le t \le t_2 \end{cases} \tag{18}$$

Where the balancing current i_{ca} is

$$i_{c1}(t) = \begin{cases} \frac{v_{c1}(t_0) - v_{ca1}(t_0)}{r} e^{-\frac{2t}{rc}} & t_0 \le t \le t_1 \\ \frac{v_{c2}(t_1) - v_{ca1}(t_1)}{r} e^{-\frac{2(t-t_1)}{rc}} & t_1 \le t \le t_2 \end{cases} \tag{19}$$

According to (16-19), the voltage difference between C_1 & C_2 will decrease after a number of ping-pong operations.

Figure 7 shows the control scheme for the auxiliary circuit. This control scheme is generating PWM pulses for auxiliary circuit switches by comparing a signal of constant magnitude with triangular carrier wave such that S2 & S4 are the complimentary of S1& S3 respectively for carrying out ping-pong operation.

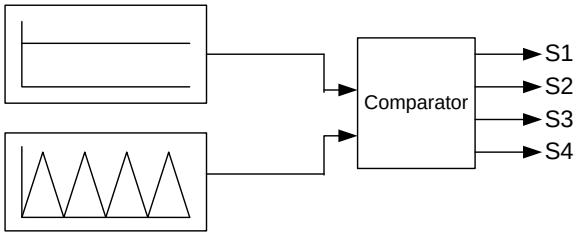


Figure 7. Control Scheme for auxiliary circuit.

4. Result and Discussion

In this section, simulation results are presented and verified experimentally by developing laboratory prototype of neutral point clamped (NPC) active front end (AFE) 3-level converter.

A. Simulation Results

Simulation results are given for evaluating the performance of the neutral point clamped (NPC) active front end (AFE) 3-level converter using UPC. The simulation is carried out with and without NPP regulator in the UPC under balanced and unbalanced load conditions. The block diagram of simulation model is shown in Figure. 8 and simulation parameters are given in Table 2. The optimized controller parameters are given in Table 3.

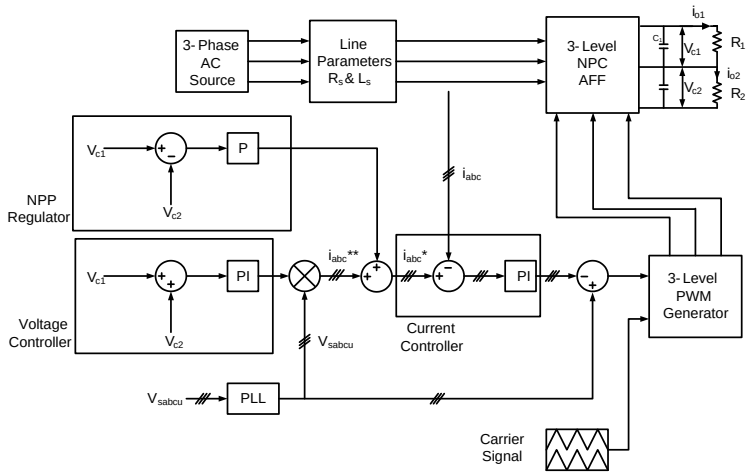


Figure. 8 Block diagram of neutral point clamped active front end 3-level converter with UPC

Table 2. Simulation Parameters for NPC AFE 3-Level Converter with UPC

Line Voltage (RMS)	V_{LL}	50 V
Boost Inductor	L_s	7.73mH
AC Link Resistance	R	0.1 Ω
DC Link Voltage	V_{dc}	80 V
DC Link Capacitance	C_1/ C_2	2200 µF
Load Resistance	$R_1 \parallel R_1'$	15 Ω ‖ 15 Ω
	$R_2 \parallel R_2'$	15 Ω ‖ 15 Ω
Carrier Frequency	f_c	2050 Hz

Table 3. Selected UPC Parameters for NPC AFE 3-Level Converter

Current Controller Parameters	
Proportional Gain (K_{cp})	0.5
Integral Gain (K_{ci})	10
Voltage Controller Parameters	
Proportional Gain (K_{vp})	2
Integral Gain (K_{vi})	25
NPP Regulator Parameters	
Proportional Gain (K_{np})	2

A.1 Performance of NPC AFE with UPC

Phase voltage of phase 'a', line current of phase 'a', dc link capacitor voltages (V_{c1} and V_{c2}) and load current (i_0) under steady state condition is shown in Figure. 9. This shows the stable operation of neutral point clamped active front end 3-level converter with unity power factor controller under steady state condition, which is essentially required for medium voltage, high power applications.

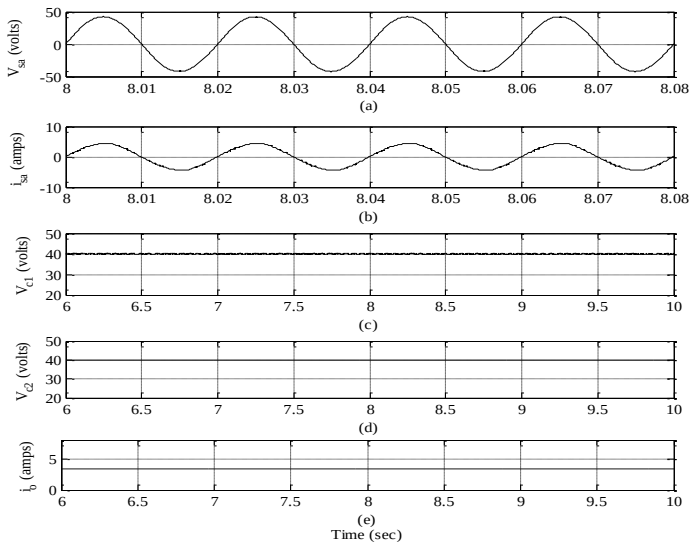


Figure 9. Phase voltage (V_{sa}), Line current (i_{sa}), dc link capacitor voltages (V_{c1} and V_{c2}) and load current (i_0) of NPC AFE 3-level converter under steady state condition

The dynamic performance of NPC AFE AC-DC converter is also evaluated with sudden load change as shown in Figure. 10 & Figure. 11. It is observed that the dc link capacitor voltages (V_{c1} and V_{c2}) settled down to its desired value within 10 cycles, the supply

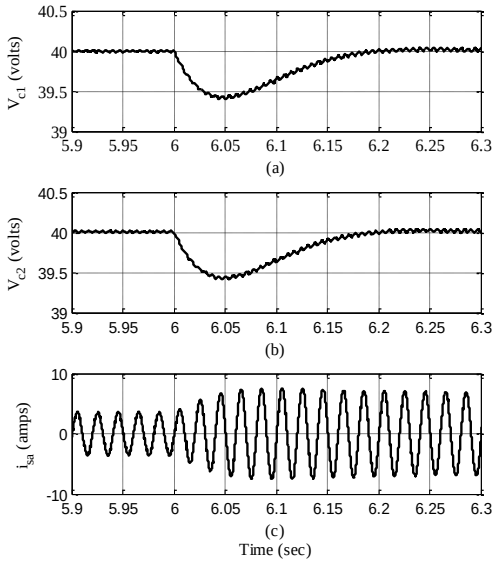


Figure 10. DC link Capacitor Voltages (V_{c1} and V_{c2}) , DC link Capacitor Voltage (V_{c1}) and Source current (i_{sa}) for increase in load at t = 5 sec

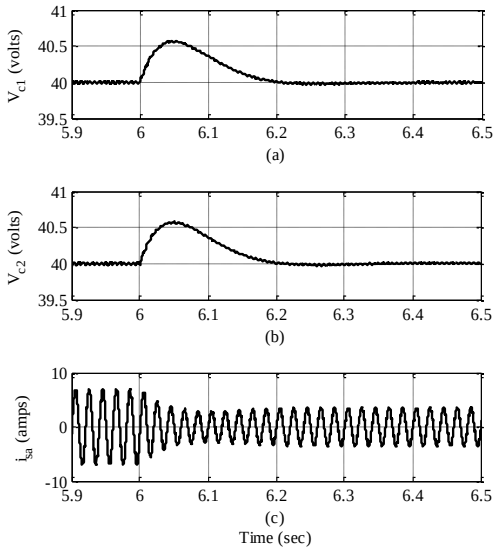


Figure 11. DC link Capacitor Voltages (V_{c1} and V_{c2}) , DC link Capacitor Voltage (V_{c1}) and Source current (i_{sa}) for decrease in load at t = 10 sec

A.2. Neutral Point Potential (NPP) Control Using NPP Regulator

The neutral point potential is basically difference between two dc link capacitor voltages. Ideally NPP should be zero i.e. balanced dc link capacitor voltages under transient and steady state conditions. In this study, simulation is carried out with and without NPP regulator in UPC under balanced and unbalanced load condition. The level of unbalance is measured by a factor defined as depth of unbalance σ as [27]

$$\sigma = \frac{R_1 - R_2}{R_1 + R_2} \times 100 \quad (20)$$

Where R_1 load resistance is across dc link capacitor C_1 and R_2 is load resistance across dc link capacitor C_2.

The study is carried out for different depth of unbalance (σ) to observe its effect on the performance of NPP regulator in UPC. The system parameters for the simulation are same given in Table 2. The details of loading parameters are given in Table 4

Table 4. Load Parameters

Resistance (R_1) (Ω)	Resistance (R_2) (Ω)	% Depth of unbalanced load (σ)
15	15	0
15	10	20
15	7.5	33.33

Figure 12 shows the NPP variation with and without NPP regulator. It clearly shows that there are variations in average of NPP under balanced load (σ = 0%). Even though the variation is not large, but it is significant for high voltage and high power applications. When NPP regulator is included in the UPC, the NPP variations got suppressed and NPP become almost zero as shown in the Figure. 12. Figure. 13 and Figure. 14 shows the variations of NPP with and without NPP regulator in UPC for σ = 20% and σ = 33.33% respectively. These Figure shows that the variations of NPP increases with depth of unbalance. The NPP regulator in UPC is capable to control the NPP variations as shown in Figure. 13 and Figure. 14.

Figure. 15 shows the dc link capacitor voltages (V_{c1} & V_{c2}) before and after the NPP regulator included in the UPC. It also confirms the balancing of dc link capacitor voltages using NPP regulator in UPC.

Table 5 shows that, the NPP regulator in UPC removes the 2nd harmonic from supply line current whereas the dc off-set appears in the supply line current as depth of unbalance increase. The undesirable dc off-set in supply current will saturate the transformer on the utility side and must be removed from the supply current. Therefore, the NPP regulator in the UPC controls the variations in NPP under balanced load whereas for different depth of unbalance the NPP regulator able to control NPP variations at the cost of dc off-set in supply line current.

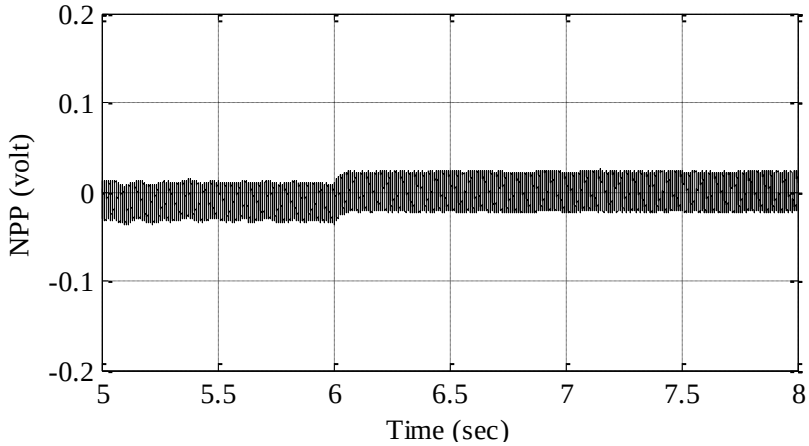


Figure 12. NPP before and after NPP regulator is included in UPC at t = 6 sec for σ = 0%

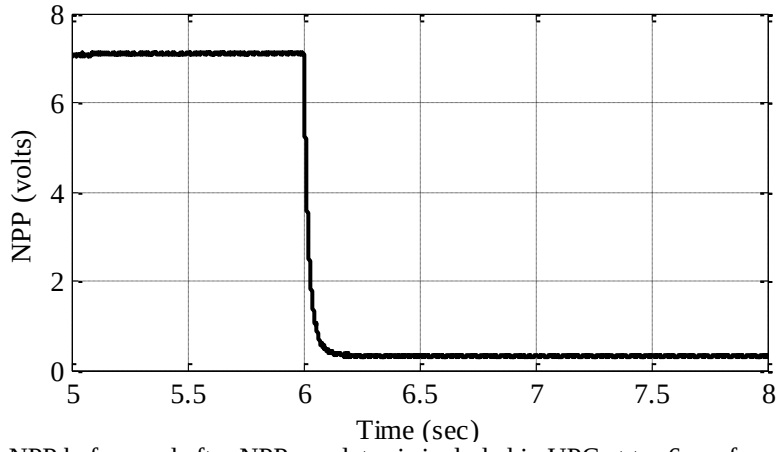


Figure 13. NPP before and after NPP regulator is included in UPC at t = 6 sec for σ = 20%

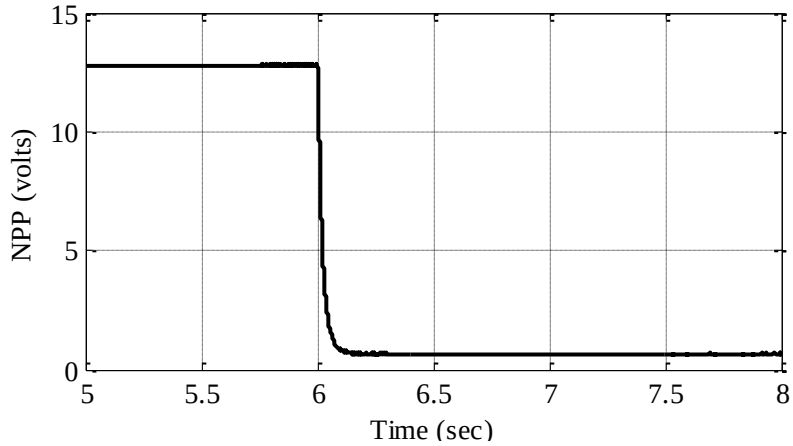


Figure 14. NPP before and after NPP regulator is included in UPC at t = 6 sec for σ = 33.33%

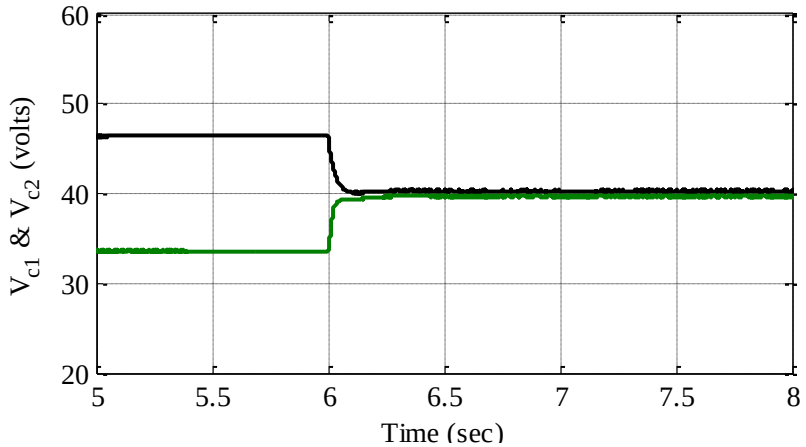


Figure 15. DC link capacitor voltages (V_{c1} & V_{c2}) before and after NPP regulator is included in UPC at t = 6 sec for σ = 33.33%

Table 5. Variation of DC offset & 2nd Harmonic with depth of unbalance (σ) in Supply Line Current of Phase a (i_{sa}) with and without NPP Regulator in UPC

Depth of Unbalance (σ)	DC Off-set and 2nd Harmonic in Supply Line Current of Phase a (i_{sa})			
	Without NPP Regulator		With NPP Regulator (%)	
	DC Off-set (%)	2nd Harmonic (%)	DC Off-set (%)	2nd Harmonic (%)
0%	0	0	0	0
20%	0	10	15%	0
33.33%	0	17	25%	0

A.3. Neutral Point Potential (NPP) Control Using Auxiliary Circuit

A simulation has been carried out for AC-DC multilevel converter with an auxiliary circuit for σ = 33.33%. As shown in Figure.16 the average NPP is become almost zero when auxiliary circuit is included at t = 6 sec. Figure.17 shows the voltage across the dc link capacitors (V_{c1} & V_{c2}) before and after the auxiliary circuit is included in system. The simulation confirms that the adopted voltage balancing scheme using auxiliary circuit is maintaining almost equal voltage across the dc link capacitors. Table 6 also shows that the auxiliary circuit balances dc link voltage without dc offset in the input line current for different depth of unbalance load.

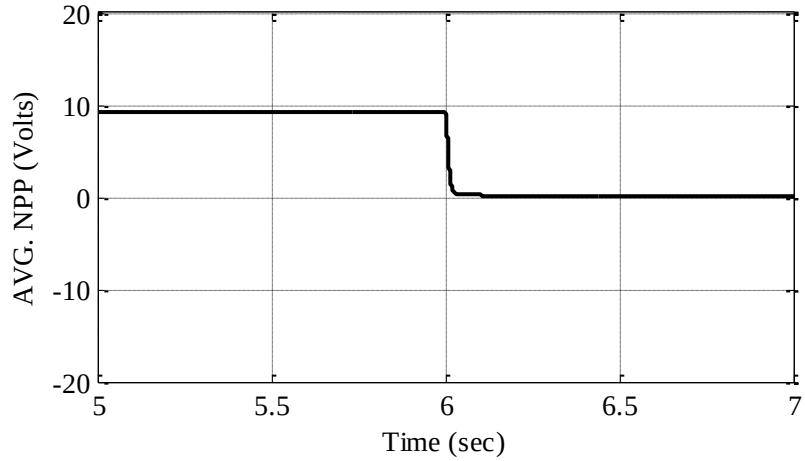


Figure 16. Average NPP when auxiliary circuit is included at t = 6 sec for σ = 33.33%

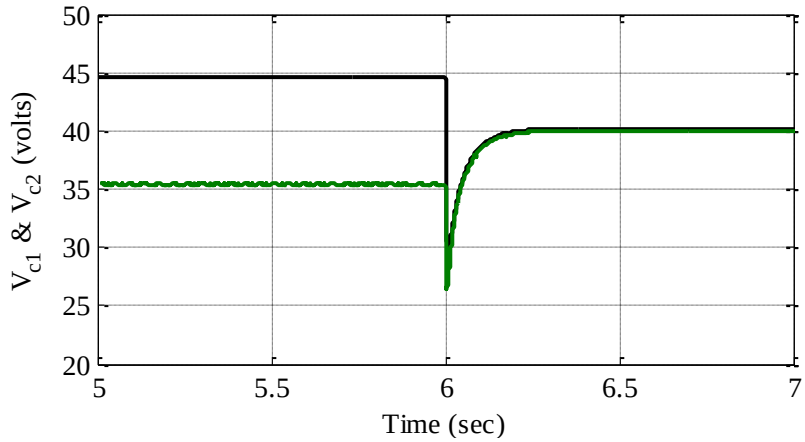


Figure.17 DC link voltages (V_{c1} & V_{c2}) when auxiliary circuit is included at t = 6 sec for σ = 33.33%

Table 6. Variation of DC offset & 2nd Harmonic with depth of unbalance (σ) in Supply Line Current of Phase a (i_{sa}) with Auxiliary Circuit

Depth of Unbalance (σ)	DC Off-set and 2nd Harmonic in Supply Line Current of Phase a (i_{sa}) with Auxiliary Circuit	
	DC Off-set (%)	2nd Harmonic (%)
0%	0	0
20%	0	0
33.33%	0	0

B. Experimental Results

The performance of NPC AFE 3-level converter is verified experimentally on developed low power prototype in laboratory. The experimental parameters for NPC AFE 3-level converter are given in Table 7. The prototype of AC-DC converter includes twelve STGW30N120KD, 1200 volts, 30 amps IGBTs and six fast recovery diodes (16FM120) with two dc link capacitors of 2200mF, 600 V each at input side. The control algorithm is implemented through dSPACE real time interface DS1103. The DS1103 real time hardware implementation board is based upon Texas Instruments TMS320F240, 16 bit fixed point digital signal processor, 250 MHz CPU, 20 MHz clock frequency.

Table 7. Experimental Parameters

Line Voltage (RMS)	V_{LL}	50 V
Source Inductor	L_s	7.73mH
AC Link Resistance	R	0.4 Ω
DC Link Parameters		
DC Link Voltage	V_{dc}	80 V
DC Link Capacitors	C_1 and C_2	2200 μF
Load Parameters		
Load Resistance	(R_1 and R_2)	15 Ω
Carrier Frequency	f_c	2050 Hz

B.1. Performance of NPC AFE with UPC

The line voltage (V_{ab}) at supply end, supply phase voltage (V_{sa}) and line current (i_{sa}) are shown in Figure. 18, which clearly shows unity power factor operation of the converter. The harmonic profile of the line voltage (V_{ab}) at supply end and line current (i_{sa}) are shown in Figure. 19 (a) and Figure. 19 (b) respectively. The line current (i_{sa}) drawn by NPC AFE 3-level converter is having only 2.4% of THD, which is well below the limit imposed by standard IEEE 519.

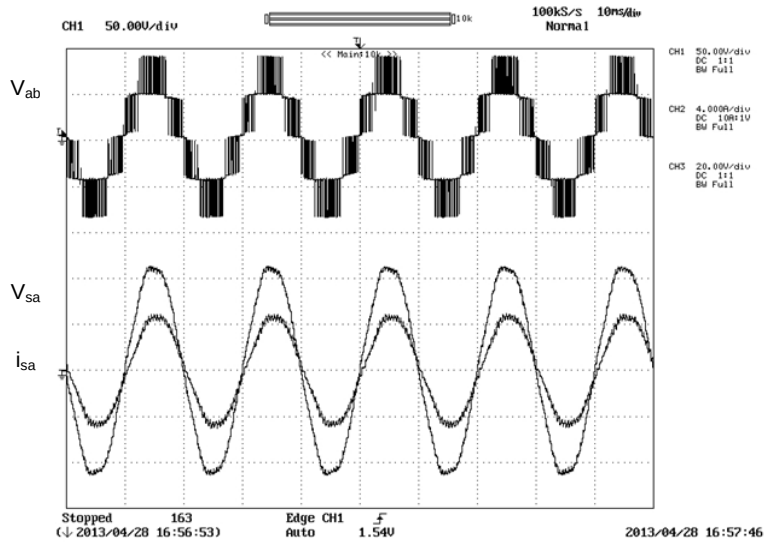
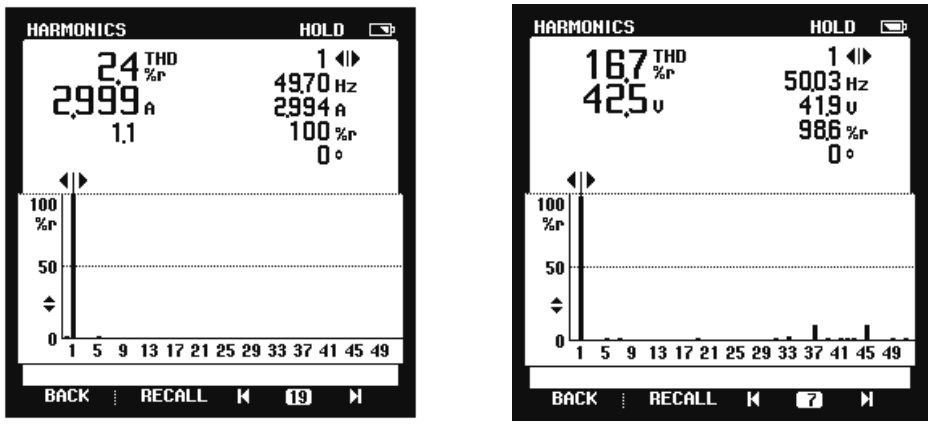


Figure 18. Converter line voltage (V_{ab}), phase voltage (V_{sa}) and line current (i_{sa}) of NPC AFE 3-level converter

X - axis: Time – 10ms/div, Y axis: V_{ab} - 50 V/div, V_{sa} – 20V/div and i_{sa} – 4A/div



(a) (b)

Figure.19 Harmonic spectrum of (a) Line current (i_{sa}) and (b) converter line voltage.

The performance of NPC AFE 3-level converter under steady state condition has been verified experimentally. The phase voltage (V_{an}) at supply end is shown in Figure. 20 under steady state condition which confirms one of the important features of multilevel converter having half of the dc link voltage subjected across the devices. The voltage across the dc link capacitors (V_{c1} and V_{c2}) are shown in Figure. 21 under steady state condition. This shows stable operation of converter under steady state condition.

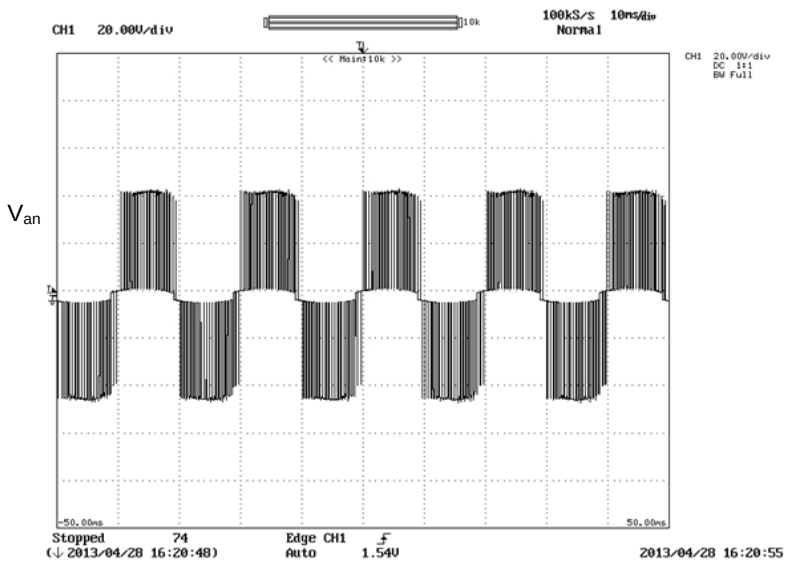


Figure 20. Phase voltage (V_{an}) at supply end of NPC AFE 3-level converter under steady state condition

X - axis: Time –10ms/div, Y - axis: V_{an} - 20 V/div

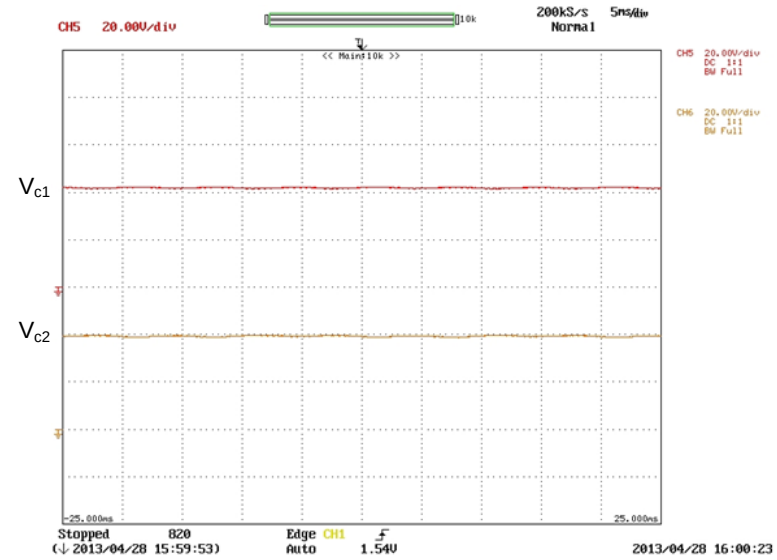


Figure 21. DC link capacitor voltages (V_{c1} and V_{c2}) of NPC AFE 3-level converter under steady state condition

X axis: Time- 10ms/div, Y axis: V_{c1} and V_{c2} - 20 V/div

The transient response of the converter is evaluated with sudden change in load. The dc link voltages (V_{c1} and V_{c2}) and line current of phase 'a' (i_{sa}) has been observed when load is suddenly increased as shown in Figure.22. It can be clearly observed that the dc link voltages (V_{c1} and V_{c2}) decreased when load is suddenly increased thereafter few cycles the dc link voltages recover to its desired voltage. The behaviour of the converter is also observed when load is reduced. The

dc link voltages suddenly increased and after few cycles it gets back to its desired value, shown in Figure.23. The response of the NPC AFE 3-level converter during transient found satisfactory with UPC, and confirmed that UPC is effectively able to regulate dc link voltage quickly at desired value during transient condition

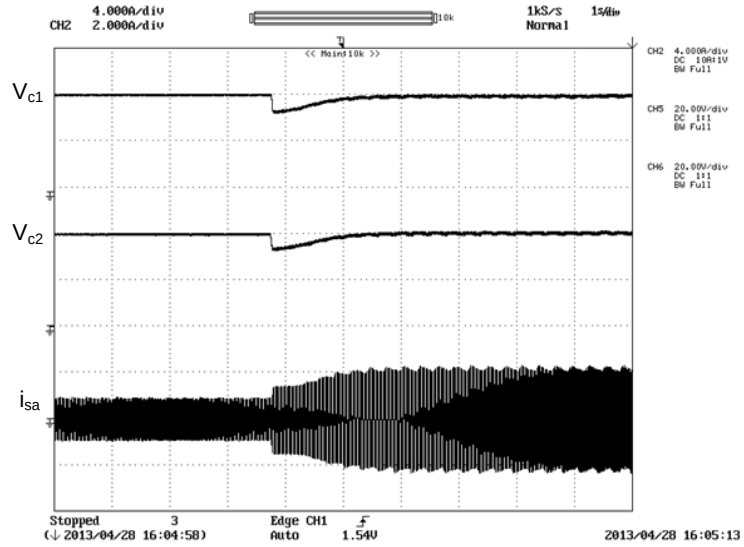


Figure 22. DC link capacitor voltages (V_{c1} and V_{c2}) and line current (i_{sa}) of NPC AFE 3-level converter when load is increased

X - axis: Time – 1s/div, Y - axis: V_{c1} and V_{c2} - 20 V/div, i_{sa} – 4 A/div

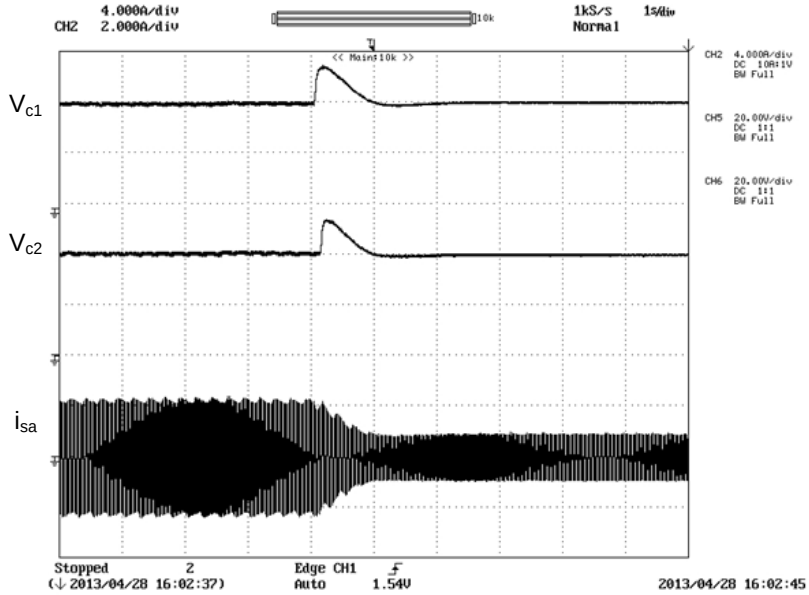


Figure.23 DC link capacitor voltages (V_{c1} and V_{c2}) and line current (i_{sa}) of NPC AFE 3-level converter when load is decreased

X - axis: Time – 1s/div, Y- axis: V_{c1} and V_{c2} - 20 V/div, i_{sa} – 4 A/div

B.2 Neutral Point Potential (NPP) Control with NPP Regulator in UPC

It is experimentally verified that multilevel structures have inherent problem of NPP variation. Figure. 24 shows variation of NPP before and after the NPP regulator included in t = 3 sec for σ = 33.33%, which verifies the effective working of NPP regulator in UPC.

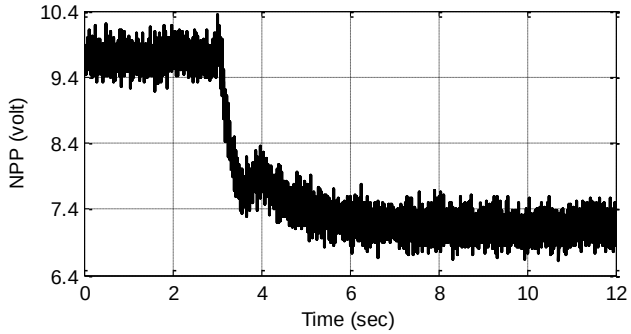


Figure 24. NPP variation before and after NPP regulator included in UPC at t = 3 sec for σ = 33.33% (Control Desk Layout)

B.3 Neutral Point Potential (NPP) Control with Auxiliary Circuit

The function of auxiliary circuit has also been verified experimentally. Figure. 25 shows the dc link capacitor voltages (V_{c1} & V_{c2}) before and after auxiliary circuit included in the system for σ = 33.33%. As shown in the Figure. 25 the dc link capacitors voltages are not completely balanced because of series resistance r is connected with auxiliary capacitor C_a to limit the amplitude of the charging current for practical consideration. The presented result confirms the working of auxiliary circuit adopted to balance the dc link capacitors voltage.

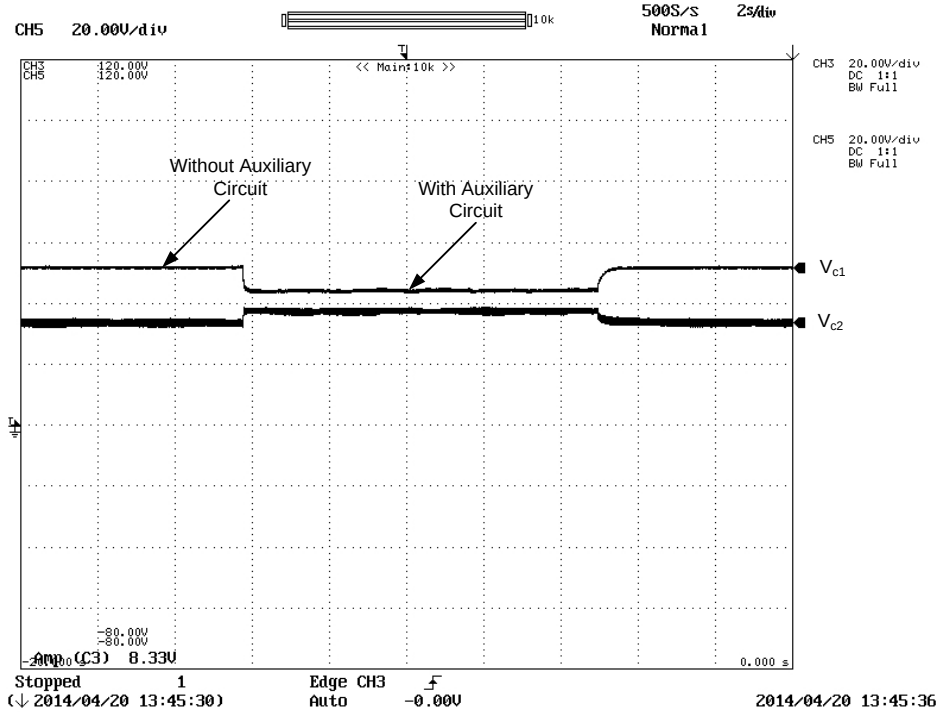


Figure 25. DC link capacitor voltages (V_{c1} and V_{c2}) before and after auxiliary circuit included in the system for σ = 33.33%

X - axis: Time – 1s/div, Y- axis: V_{c1} and V_{c2} - 20 V/div

4. Conclusion

The unity power factor controller (UPC) is presented to control NPC AFE 3-level converter for improved power quality at input and load side. The performance of three-phase NPC AFE 3-level converter has been evaluated with unity power factor controller. Simulation results are presented to study the performance of the system during transients as well as in steady state. It is observed that 3-level converter is operating at almost unity power factor with supply current THD within the limits imposed by IEEE519 standard. Simulated results also show that NPP regulator in conjunction with UPC is able to balance the capacitor voltages under balanced and unbalanced load with the addition of dc off-set in supply line current. The simulation results with an auxiliary circuit to balance the dc link capacitor voltages show effective balancing of dc link capacitor voltages without any adverse effects in terms of power quality. The features of UPC with NPP regulator and auxiliary circuit, observed in simulation study are also validated through experimentation performed on the low power prototype developed in laboratory using dSPACE DS 1103. Further, it can be concluded that the UPC with NPP regulator is suitable for drives application where depth of unbalance is not much whereas an auxiliary circuit is effective for active power filter where depth of unbalance is high.

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