Two High Slew Rate Buffers Based on Flipped Voltage Follower

Mona Khanjani Moaf, Milad Piri, and Parviz Amiri

Department of Electrical Engineering
Khatam Institute of Higher Education
Tehran, Iran.

Abstract: Two Voltage followers (VF) suited to low-voltage operation and able to operate with a high-slew rate and low-output impedance are presented. The buffer core is based on the flipped voltage follower (FVF) which is previously presented in literature. A detailed comparison of proposed buffers and other voltage followers is presented. These buffers have been simulated using 0.18 µm CMOS technology models provided by TSMC. The buffers consume 10 µA from 1.2 V supply and have a power consumption of 25 µw. The first and second proposed buffers have slew rate of 13 V/µs and 32 V/µs, respectively, with output impedance of about 50 Ω.

Keywords: high-slew rate, low-output impedance, buffer, flipped voltage follower, class-AB.

1. Introduction

The conventional VF shown in Figure 1(a) is one of the basic building blocks of analog VLSI systems; it is biased on the source side with a constant current source I_b which ideally keeps a constant gate-to-source voltage in M1. This causes output voltage variations to follow the input voltage with a gate-source DC level shift [1, 2]. In this circuit the sourcing current capability is limited by the current source I_b. In practice this VF suffers from high-output impedance, dependence of drain current of M1 on the output current, and nonsymmetrical slew rate.

The FVF shown in Figure 1(b) [3] is an improvement to the conventional VF, due to use of feedback which increases the output conductance and consequently bandwidth. It is worth mentioning that the latter is limited by a large capacitive load [4]. In this circuit the sinking current capability is limited by the current source I_b. Thus it doesn’t operating in class-AB mode.

Class-AB circuits are characterized by low quiescent power consumption and high driving capability, taking current from the supply sources only when the load requires it. Therefore class-AB circuits are considered to be good candidates for low-power analog design [5, 8, 9, 10, and 11].

The circuit of Figure 1(c) is the class-AB FVF [5]. Under quiescent conditions the current through transistor M2 is equal to I_b and transistor M4 copies the current of transistor M1, as they share the gate and the source terminals. Therefore the current taken from the transistor M2 is 2I_b. The stability of this circuit is determined by the stability of the FVF (Figure 1(b)). If the current source I_b is implemented by means of a simple current mirror, the stability condition leads to [3]:

$$\frac{C_X}{C_Y} < \frac{g_{m1}}{4g_{m2}}$$

(1)

where C_X and C_Y are the equivalent capacitances at nodes X and Y, respectively. For small capacitive loads this condition is achieved by proper sizing of M1 and M2.

In this paper a very simple technique is used to increase slew rate and output conductance, while the power consumption is kept constant.

Received: February 15th, 2015. Accepted: June 20th, 2016
DOI: 10.15676/ijeei.2016.8.2.15
In section 2 the first circuit is proposed in which the slew rate and output conductance are increased. The second proposed buffer is presented in section 3 in which the slew rate increases excessively. In section 4 proposed structures and other buffers have been simulated using the models of the TSMC 0.18 µm technology, and in section 5 a comparison of buffers in terms of output impedance, slew rate, voltage gain, total harmonic distortion, and power consumption is presented.

The proposed structure has been simulated using the models of the TSMC CMOS 0.18µm technology, in order to compare its performance with the other buffers in terms of settling time, bandwidth, output impedance, power consumption, and total harmonic distortion (THD).

![Voltage follower](image)

Figure 1. Voltage follower: (a) Conventional VF [1]. (b) FVF [3]. (c) Class-AB FVF [5].

2. First Proposed buffer

This new unity-gain buffer shown in Figure 2(a) is able to source and sink a maximum current which is higher than its quiescent current, providing Class-AB operation. In quiescent conditions the current through transistors M4 and M2 is equal to \(I_b\) and \(2I_b\), respectively.
When the input signal $V_{in}$ increases, with respect to the output voltage $V_o$, the source-to-gate voltage of transistor M1 tends to decrease. As transistor M1 is biased by the current source $I_b$, its drain-to-source voltage increases forcing a large current through transistor M2, and leading the transistor M4 into the cut-off region. In this operation regime, the current delivered to the output load is given by:

$$I_{out} = I_{D_2} - I_b - I_{D_4}$$  \hspace{1cm} (2)

As explained above, the first and the third parameters in Equation (2) ($I_{D_2}$ and $I_{D_4}$) increases and decreases, respectively; while in the circuit of Figure 1(c), when the input signal increases the output current is equal to $I_{D_2} - 2I_b$ in which only the first parameter ($I_{D_2}$) increases. Thus the positive slew rate in this proposed buffer improves.

When the input voltage decreases, transistor M1 tends to the ohmic region. As the current through M1 is fixed to the current source of $I_b$, its source-to-drain voltage decreases leading the transistor M2 into the cut-off region. On the other hand, transistor M4 whose source voltage is fixed to the ground, sinks a large current from the output load. In this operation regime the current drained from the output load is given by:

$$I_{out} = I_{D_4} + I_b - I_{D_2}$$  \hspace{1cm} (3)

As explained above, the first and third parameters in Equation (3) ($I_{D_4}$ and $I_{D_2}$) increases and decreases, respectively; while in the circuit of Figure 1(c) when the input voltage decreases, the output current is given by $2I_b - I_{D_2}$ in which only the second parameter ($I_{D_2}$) decreases. Thus, in this proposed buffer, the negative slew rate improves too. Thus, the proposed buffer has better performance in term of slew rate.

In quiescent conditions, the gate-to-source voltage of transistor M4 is given by:

$$V_{GS4} = V_{DD} - V_{SG2} = V_{DD} - \sqrt{\frac{I_{D_2}}{K_2}} - V_{thp}$$  \hspace{1cm} (4)

In Equation (4) notation $K_2$ is $\frac{1}{2} \frac{\mu pC_mW}{L}$. To turn on the transistor M4, the minimum supply voltage required is given by:

$$V_{DD} \geq V_{thp} + \sqrt{\frac{I_{D_2}}{K_2}} + |V_{thp}|$$  \hspace{1cm} (5)

To decrease the required supply voltage, a DC level shifter shown in Figure 2(b) can be employed. In this circuit the Equation (5) is given by:

$$V_{DD} \geq V_{thp} + \sqrt{\frac{I_{D_2}}{K_2}} + |V_{thp}| - V_L$$  \hspace{1cm} (6)

The implementation of this DC level shifter is discussed in [6] and [7], and it is shown in Figure 2(c).

The minimum voltage required to keep M1 in saturation is given by:

$$V_{in} \geq V_{G2} - |V_{thp}|$$  \hspace{1cm} (7)

Also the condition of saturation for transistor M4 is given by:

$$V_{in} \geq V_{G2} + V_L - V_{SG1} - V_{thq}$$  \hspace{1cm} (8)

From Equations (7) and (8), it can be concluded that decreasing the input signal leads the transistor M1 into the ohmic region before the transistor M4, thus the transistor M4 doesn’t limit the input signal range.
Figure 2. First proposed circuit: (a) Basic implementation. (b) Improved by DC level shifter. (c) DC level shifter implemented based on [6, 7]. (d) Open-loop gain analysis of circuit of (a).
Figure 2(d) shows the same circuit with the feedback loop opened at the gate of M2 and including a test voltage source. This circuit has an open-loop gain of:

$$A_{OL} = \frac{V_o}{V_t} = \frac{-g_{m2}R_{OLY}}{1 + g_{m4}R_{OLY}}$$  \hspace{1cm} (9)

where the open-loop resistance at node Y is given by $R_{OLY} = r_b \parallel g_{m1}r_\alpha r_\beta$, and the notation $g_m$ is small signal transconductance. The open-loop resistance at node X is given by:

$$R_{OLX} = \frac{1}{g_{m1}[1 + (g_{m4} - \frac{1}{r_\alpha}(r_b \parallel r_\beta))] \parallel r_\beta}$$  \hspace{1cm} (10)

The closed-loop resistance at node X is given by $R_{CLX} = R_{OLX}/(1 + |A_{OL}|)$. If the current source $I_b$ is a simple current source ($r_b = r_\alpha$) $R_{CLX}$ tends to:

$$R_{CLX} = \frac{2}{g_{m1}r_\alpha (g_{m2} + g_{m4})}$$  \hspace{1cm} (11)

This is lower than the output impedance of circuit of Figure 1b which is equal to $2/g_{m1}g_{m2}r_\alpha$ [3].

In order to ensure stability, the condition $\omega_{px} > 2GB$ must be satisfied [3]. (Where the high-frequency pole at node X is given by $\omega_{px} = 1/R_{OLX}C_X$, the dominant pole at node Y, $\omega_{py} = 1/C_YR_{OLY}$, and the gain-bandwidth product, $GB = g_{m2}/[c_1(1 + g_{m2}R_{OLY})]$) For $r_b = r_\alpha$, this condition leads to

$$\frac{C_X}{C_Y} < \frac{r_\alpha g_{m1}(1 + r_\alpha g_{m4})}{4}$$  \hspace{1cm} (12)

This condition is much more easily achieved by proper sizing of transistor M1 and M4 than the condition of Equation (1). Thus this proposed circuit is good candidate for driving large capacitor loads.

3. The Second Proposed Circuit

In the circuit of Figure 1(c) transistor M4 senses the voltage variations at the gate of transistor M1 and improves the current sinking capability. In the circuit of Figure 2(a), transistor M4 senses the voltage variations at the drain of transistor M1, and it improves the current sinking capability. If we design a circuit in which both above techniques are used, the slew rate will improve. This circuit is shown in Figure 3.

Under quiescent conditions, the current through transistors M2, M7, and M5 is equal to $2I_b$, $0.5I_b$, and $I_b$, respectively. The bias current of M4 is kept small so that M4 operates in subthreshold region.

When the input signal increases the current delivered to the output load is given by:

$$I_{out} = I_2 + I_7 - I_b - I_5$$  \hspace{1cm} (13)

In this operation regime the current through transistors M4 and then M7 decreases; and because of voltage increase at node Y, the current through transistors M5 and M2 increases and decreases, respectively. Thus in the Eq. (14) the first parameter ($I_3$) increases and the last two parameters ($I_2$ and $I_7$) decrease, so the current sinking from the load increases more in comparison with the circuit of Figure 2(a).
When the input signal decreases, the output current sinking from the load is given by:

\[ I_{\text{out}} = I_5 + I_b - I_2 - I_7 \]  \hspace{1cm} (14)

From Equations (13) and (14) it can be observed that when the input signal variations are large, three parameters \(I_2, I_7,\) and \(I_5\) change excessively, while in the circuit of Figure 2(a), only two parameters change, and in the circuit of Figure 1(c), only one parameter changes. Thus the slew rate in this proposed buffer improves significantly.

Table 1. Devices sizing

<table>
<thead>
<tr>
<th>MOS Width (µm)</th>
<th>First proposed circuit</th>
<th>Second proposed circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-</td>
<td>M6</td>
</tr>
<tr>
<td>2.4</td>
<td>M4</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>M2</td>
</tr>
<tr>
<td>4</td>
<td>M3</td>
<td>M3</td>
</tr>
<tr>
<td>5.8</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>8.5</td>
<td>M2</td>
<td>-</td>
</tr>
<tr>
<td>10</td>
<td>-</td>
<td>M4</td>
</tr>
<tr>
<td>11.4</td>
<td>-</td>
<td>M5</td>
</tr>
<tr>
<td>30</td>
<td>M1</td>
<td>M1</td>
</tr>
<tr>
<td>43</td>
<td>-</td>
<td>M7</td>
</tr>
</tbody>
</table>

The voltage gain is given by:

\[
\frac{V_o}{V_{\text{in}}} = \frac{N g_{m4} + r_{o1} g_{m1} \left( g_{m2} + g_{m5} \right)}{1 + \left( g_{m2} + g_{m5} \right) \left( r_{o1} g_{m1} \right)}
\]  \hspace{1cm} (15)

where the notation \(N\) is \((W/L)_7/(W/L)_6\), and \(R_o\) is the output impedance (in this case is approximately equal to \(R_{CLX}\) in the circuit of Figure 2(a)).

In order to have unity-gain buffer the condition \(N g_{m4}=1/R_o\) must be satisfied, which is easily achieved by proper sizing of \(W/L\) ratio of transistors \(M7\) and \(M6\).

The stability of this proposed circuit is determined by the stability of circuit of Figure 2(a).

4. Simulation Results

The structures of proposed buffers (Figure 2(a) and 3) were simulated with the supply voltage of 1.2 V, which is the standard for the technology. For the simulations, 0.18 µm CMOS technology parameters were used that have nominal NMOS and PMOS threshold voltages \(V_{\text{thN}}=0.5V\) and \(|V_{\text{thP}}|=0.49V\), respectively. The biasing current source is equal to 10 µA. All the devices used have 0.5 µm length (three times the lowest value for the employed technology).
Table 1 summarizes the device widths for the topologies (where transistor M3 is the current source).

Figure 4 shows the step response of the buffers with a capacitor load of 10 pF. The input step signals of the buffers have frequency of 1MHz and 0.4 V<sub>pp</sub> swings, with the same average values which maximizes the linear range of the amplifiers. The input bias voltage of amplifiers is 0.47 V. This figure shows a slew rate of 32 V/µs for the second proposed buffer and 13 V/µs for the first proposed buffer. This result agrees with the expected slew rate. The proposed buffers have an undershoot on the falling edge and an overshoot on the rising edge, which increases the settling time.

![Figure 4. step response of buffers with input pulse of 0.4V<sub>pp</sub>](image)

Figure 5 shows the frequency response of buffers with a capacitor load of 100 pF. It can be observed that the circuits have bandwidth of 15MHz. Figure 6 shows a comparison of the (magnitude) of the output impedance obtained by applying a 1A AC current source to the buffers’ output terminals with the input grounded. It can be seen that the buffers have output impedance of 56 and 46, respectively.

![Figure 5. Frequency response of buffers with capacitor load of 100 pF.](image)
Figure 6. Output impedance of buffers.

Figure 7 shows the measured response for a 1MHz, 200 mV peak-to-peak sinusoidal input voltage. The measured THD was -45.7 and -58.6, respectively. Figure 8 shows the static large-signal gain of the buffers. It can be observed that gain of the second proposed buffer is constant over a larger input signal range than the first proposed buffer.
5. Comparison of buffers

Table 2 summarizes the simulated results of the buffers in terms of power consumption, slew rate, output resistance, voltage gain, THD, and voltage supply. Furthermore, a figure of merit is defined to compare the proposed circuits, which is given by (Slew Rate * C_L)/Power.

It can be observed that all the buffers have a power consumption of 25 µW. The proposed buffers have a higher slew rate and output conductance than the class-AB FVF[5], and the gain is about unity.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Technology</th>
<th>Voltage Supply</th>
<th>I Oc (µA)</th>
<th>Power consumption (µw)</th>
<th>Slew Rate</th>
<th>Output resistance</th>
<th>Gain (dB)</th>
<th>Bandwidth</th>
<th>THD</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>First proposed</td>
<td>0.18 µm</td>
<td>1.2V</td>
<td>10</td>
<td>25</td>
<td>32V/µs</td>
<td>56Ω</td>
<td>0</td>
<td>15MHz</td>
<td>-45.7dB</td>
<td>12.8</td>
</tr>
<tr>
<td>buffer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V_{PP}=0.2V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1MHz</td>
<td></td>
</tr>
<tr>
<td>Second</td>
<td>0.18 µm</td>
<td>1.2V</td>
<td>10</td>
<td>25</td>
<td>13V/µs</td>
<td>46Ω</td>
<td>-0.8</td>
<td>15MHz</td>
<td>-58.6dB</td>
<td>5.2</td>
</tr>
<tr>
<td>proposed</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V_{PP}=0.2V</td>
<td></td>
</tr>
<tr>
<td>buffer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1MHz</td>
<td></td>
</tr>
<tr>
<td>Buffer[5]</td>
<td>0.5 µm</td>
<td>1.5V</td>
<td>20</td>
<td>36</td>
<td>6.1V/µs</td>
<td>220</td>
<td>-0.2</td>
<td>87 MHz</td>
<td>-55dB</td>
<td>1.69</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C_{L}=10pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V_{PP}=0.2V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1MHz</td>
<td></td>
</tr>
<tr>
<td>Buffer[4]</td>
<td>65 nm</td>
<td>1.2V</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>760Ω</td>
<td>-0.4</td>
<td>100MHz</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C_{L}=2pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V_{PP}=0.2V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1MHz</td>
<td></td>
</tr>
<tr>
<td>FVF[3]</td>
<td>65 nm</td>
<td>1.2V</td>
<td>7.8</td>
<td>-</td>
<td>-</td>
<td>540Ω</td>
<td>-0.6</td>
<td>30MHz</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C_{L}=2pF</td>
<td></td>
</tr>
</tbody>
</table>

5. Conclusion

Two novel buffers proposed in this paper, were based on a modification of the flipped voltage follower (FVF) topology. They were introduced to make it work in class-AB. These circuits can be operated at a low voltage and low power. With respect to other voltage follower stages which have been analyzed in literature, proposed buffers have superior slew rate with lower output resistance. It was clear that by increasing the quiescent current, slew rate would improve, so a figure of merit was defined to compare proposed buffers precisely. The characteristics of the proposed buffers were validated by simulations.

6. References


Mona Khanjani moaf was born in 1991 in Bandar-e Anzali. She received the electrical engineering in 2013 from Shahid Rajaee Teacher Training University (SRTTU Tehran, Iran). She is currently pursuing her education to get MS. Degree in Khatam Institute of Higher Education in Control. Her research interest is design of analog integrated circuit, especially the design of low-voltage and low-power circuits.

Milad Piri was born in 1990 in Tehran. He received the electrical engineering in 2013 from Shahid Rajaee Teacher Training University (SRTTU Tehran, Iran), and MS. Degree from Sharif University of Technology in Microelectronics. His research interest is design of low-voltage and low-power analog integrated circuits, especially the design of operational amplifiers.

Parviz Amiri was born in 1970, received B.S degree from University of Mazandaran in 1994, M.S from Khajeh Nasir Toosi University (KNTU Tehran, Iran) in 1997, and his Ph.D. from University of Tarbiat Modares (TMU Tehran, Iran) (2010), all degrees in electrial engineering (electronic). His main research interest include electronic circuit design in industries. His primary research interest is RF and power circuit design. He is currently with the department of electrical engineering Shahid Rajaee Teacher Trainning University in Tehran, Iran.