Design and Implementation of Efficient Curve Tracer for Photovoltaic System under Partial Shaded Conditions

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Abstract: Photovoltaic (PV) panels are subjected to problems such as hot spots and reduced output power when operating in partially shaded conditions. Although bypass diodes are utilized to alleviate these problems, the diodes cause multiple-peak characteristics. Tracking the maximum output power in partially shaded conditions is difficult using conventional software-based maximum power point tracking (MPPT) techniques. Curve tracers can assist software-based MPPT to track the true/global maximum power point (MPP) by scanning several potential MPP areas. Therefore, a software-based MPPT with an I-V curve tracer is a preferred solution. Moreover, curve tracers reveal more about the PV array performance and the fastest method to do so.

This paper investigates the advantages and disadvantages of several I-V curve tracers and proposes a load self-adaptive PV panel characteristic curve tracer by applying a hysteretic self-controlled duty-modulated load resistor (DMLR) to a boost converter I-V curve tracer. Several advantages are achieved such as simple structure, cost-efficient implementation and no tracing limitation near the V_{oc}. A circuit for 72 W PV panel is used to verify the feasibility of the proposed curve tracer.

Keywords: Photovoltaic system, Boost Converter, Duty Modulated Load Resistor (DMLR), Curve tracer, PSpice.

1. Introduction

Awareness of the global warming and continuous increase in global electricity energy consumption has drawn attention towards the renewable energy sources. Among the renewable energy sources, power generation from solar photovoltaic (PV) system becomes more popular, because it is a clean energy source and abundant in nature. Photovoltaic panels generate direct electricity. The main problem in PV system is its non-linear characteristics which make the extraction of maximum power a difficult task. The tracking of MPP becomes more difficult because of the usage of bypass diodes in case of partially shaded PV array. PV panels are subject to problems such as hot spots and reduced output power when operating in partially shaded conditions. Bypass diodes are utilized to overcome these problems [1]-[6], but they introduce multiple peaks in the characteristics [7]-[8]. In this case, tracking of MPP is difficult using conventional software-based maximum power point tracking (MPPT) techniques [9]-[15]. Current-voltage (I-V) curve tracers can assist software-based MPPT to track the true maximum power point (MPP) by scanning several potential MPP areas. Therefore, software-based MPPT with an I-V curve tracer is a preferred solution.

Among several I-V curve tracers, boost converter I-V curve tracer has many advantages, which include simple circuit, low implementation cost and continuous input current. However, conventional boost converter I-V curve tracers have a tracing limitation near V_{oc} area [15]. To solve this problem, a load self-adaptive PV panel characteristic curve tracer is proposed by applying a hysteretic self-controlled duty-modulated load resistor (DMLR) to a boost curve tracer, called an improved boost converter I-V curve tracer [14].

In this paper, the detailed design of PV fed improved boost converter based I-V curve tracer has been discussed. The analysis has been carried out using PSpice software [16] with 72 W_P

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array. The designed circuit has been validated through hardware implementation with proposed curve tracer and the results are presented.

2. System Description

The schematic diagram of the proposed system is shown in Figure 1.

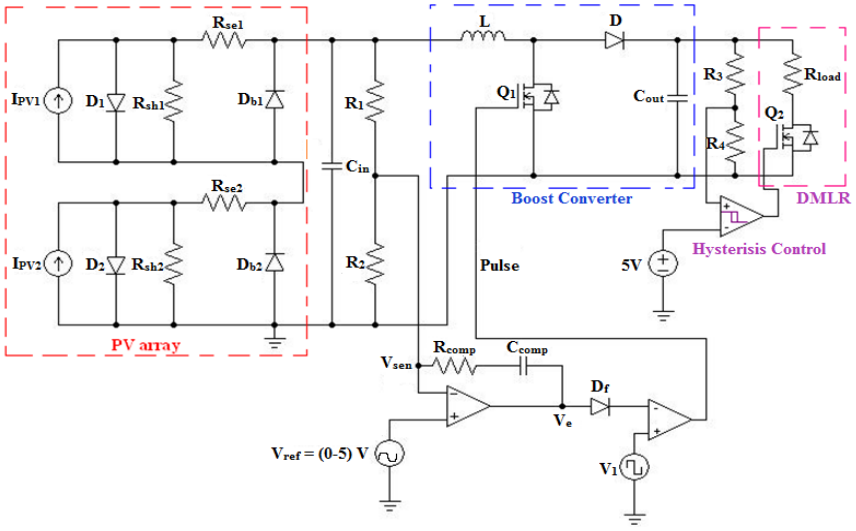


Figure 1. Schematic of the proposed system

The components of the system include a 72 WP PV array (two 36 WP panels in series), a boost converter, duty modulated load resistor (DMLR) and pulse generating circuit. A detailed design, modelling and simulation of each section in the schematic are discussed in the following sections.

A. Modelling and Simulation of PV System using PSpice

In this paper, SOLKAR make PV panel is considered. Each panel consists of 36 cells in series and the technical specifications of a single panel at standard test condition (STC: G= 1000 W/m^2, T=25^{o}C, AM =1.5 m/s) are given as; Short circuit current, I_{sc} = 2.55 A, Open circuit voltage, V_{oc} = 21.24 V, Maximum Power, P_{max} = 37.08 W, Maximum power point voltage, V_{max} = 16.54 V and Maximum power point current, I_{max} = 2.25 A. The modeling and simulation of PV panel have been carried out using PSpice software by considering one diode model of PV [15]. The parameters like shunt resistance, series resistance, diode saturation current and diode ideality factor are suitably modified to get the required characteristics. The simulation model has been validated against the panel characteristics at important points like I_{sc}, V_{oc}, V_{max}, I_{max} and P_{max}. The simulated I-V and P-V characteristics at STC are shown in Figure 2 indicating the knee points.

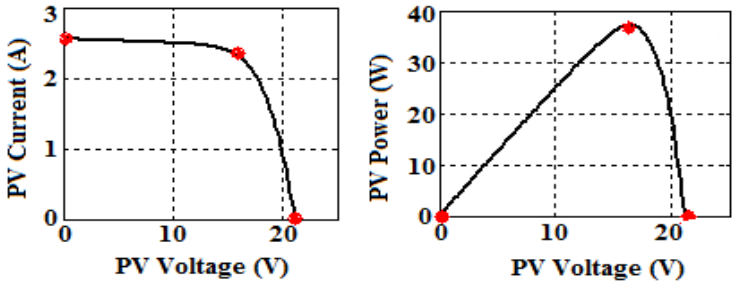


Figure 2. Characteristics of PV panel obtained using PSpice

B. Design and Simulation of an Improved Boost converter

In order to show the effectiveness of the proposed curve tracer, a small array (72 W) of two series connected panel is considered in this work. The proposed curve tracer has two parts as shown in Figure 1. The first part is boost converter with closed loop control circuit and the other part is DMLR stage containing a duty-modulated load resistor with hysteretic self-controlled circuit. The boost converter stage is same as a conventional boost V-I curve tracer where the converter pushes a panel operating point to a load operating point which has same power level. In the proposed system, a closed loop circuit forces the converter to operate at any particular operating point voltage (V_{op}) by using a proper reference voltage (V_{ref}). This loop makes the boost curve tracer more stable and controllable. As a result, accurate and flexible I-V curve tracing is achieved. The duty cycle of Q_1 is controlled by a reference signal V_{ref} with negative feedback. When the sense voltage, V_{sen} is higher than the reference voltage V_{ref}, the duty cycle of Q_1 will increase. A larger duty cycle increases the operating current of the PV panel. In the meantime, V_{sen} will reduce to trace V_{ref}. To ensure the system stability R_{comp} and C_{comp} are added. The values of sensing resistors R_1 and R_2 are calculated as in (1).

$$V_{oc} \times \frac{R_2}{R_1 + R_2} = V_{sen} \le V_{ref,max} \tag{1}$$

Where V_{oc} is the open-circuit voltage of the PV panel, $V_{ref,max}$ is the maximum value of the reference signal. $V_{ref,max}$ is chosen as 5 V here.

In Figure 1, R_{load} and Q_2 form a DMLR stage. The DMLR varies it equivalent resistance from infinite impedance to the rated resistance by adjusting its duty cycle as shown in Figure 3. It displays a new load line including three sections, the rated resistance section, transition hysteresis section, and infinite impedance section. It permits the boost converter to continuously map panel operating points to load operating points using a constant power locus mapping technique. The proposed curve tracer has two operating modes, fixed resistor (FR) and modulated resistor (MR) modes, depended on the panel's output power. In FR mode, the propose curve tracer is like a conventional boost V-I curve tracer. Q_2 always turns on and the DMLR operates in the rated resistance section. In MR mode, the DMLR modulates its equivalent resistance by adjusting the duty cycle of load switch.

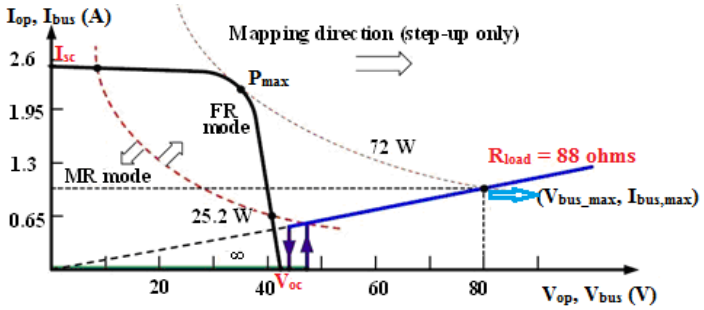


Figure 3. Load line characteristics of the proposed curve tracer

The DMLR operates in transition hysteresis section and infinite impedance section. When the proposed curve tracer scans to the V_{oc} point, Q_2 always turns off. The DMLR operates in the infinite impedance section, which means the load resistor is disconnected**.** The concept behind the hysteretic self-controlled is straightforward. Due to less power generated by the PV panels, the DMLR maintains the bus voltage between V_{bus_L} and V_{bus_H}. When the bus voltage exceeds V_{bus_H}, Q_2 turns on to let the bus capacitor discharged. On the other hand, when the bus voltage drops to V_{bus_L}, Q_2 turns off to let bus capacitor recharged as shown in Figure 4 [14].

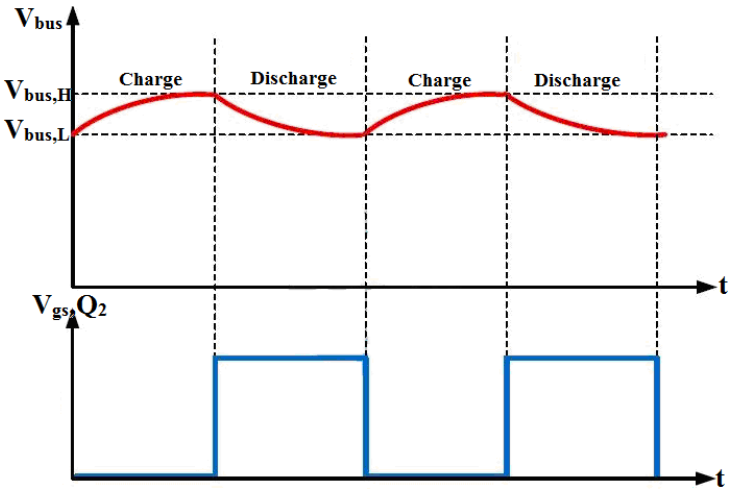


Figure 4. Waveforms of V_{bus} and V_{gs_Q2}

This hysteretic self-controlled circuit is simple and easy to be accomplished by applying a comparator LM 393 with a positive feedback loop. An op-amp μA 741 is supplied by 15 V and a reference voltage is 5 V. The value of R_3, R_4, and R_5 can be calculated as follows:

$$V_{bus\_H} = 5 \times \frac{R_3 + \left(\frac{R_4 R_5}{R_4 + R_5} \right)}{\left(\frac{R_4 R_5}{R_4 + R_5} \right)} \tag{2}$$

$$V_{bus\_L} = \left[\frac{R_3 + \left(\frac{R_4 R_5}{R_4 + R_5} \right)}{\left(\frac{R_4 R_5}{R_4 + R_5} \right)} \right] + \left[(5-15) \times \frac{R_5 + \left(\frac{R_4 R_3}{R_4 + R_3} \right)}{\left(\frac{R_4 R_3}{R_4 + R_3} \right)} \right] \tag{3}$$

C. Calculation of Hysteretic Bounds and Maximum Bus Voltage

The maximum power of PV array is 72 W, so that the proper switching frequency f_s is chosen as 50 kHz. In order to provide a stable bus voltage at MR mode, V_{bus_H} is chosen as 110 % of the V_{oc} and V_{bus_L} is chosen as 105 % of the V_{oc}. Using (2) and (3), the designed values of bus voltages are V_{bus_H} = 47 V and V_{bus_L} = 45 V. The hysteretic range of bus voltage is 2 V. Moreover, the maximum power point (MPP) under full irradiance is almost at the middle of I-V curve. Therefore, D_{Q1_pmax} is chosen between 50 % and 60 %. A larger D_{Q1_pmax} is preferred because a higher bus voltage can not only narrow MR region but also reduce the conduction loss on the diode and load switch. For these considerations, the range of bus voltage is between 68.8 V to 86 V. The maximum bus voltage V_{bus_max} is chosen as 80 V (as shown in Figure 3), so that a 100 V voltage rating electrolytic capacitor can be used as the output capacitor. The diode and the MOSFET are selected so that they can withstand 100 V [14].

D. Calculation of Load Resistor and Boundary Power

After determining the V_{bus_max}, the load resistor is chosen. Assuming the efficiency of boost converter is 100 %. The value of load resistor R_{load} is found by energy balance principle.

$$R_{load} = \frac{V_{bus\_max}^2}{P_{max}} \tag{4}$$

Where V_{bus_max} is 80 V, P_{max} is 72 W, and R_{load} is 88 Ω. The maximum power dissipation of load resistor is chosen as 90 W with 20 % de-rating. After R_{load} is chosen, $P_{boundary}$ between FR mode and MR mode is calculated as follows.

$$P_{boundary} = \frac{V_{bus\_H}^2}{R_{load}} \tag{5}$$

$P_{boundary}$ is 25.2 W (35 % of P_{max}). When the PV power exceeds 35 % of P_{max}, the improved boost converter based I-V curve tracer operates in FR mode. Otherwise, it operates in MR mode. Under full irradiance, the operating voltage at MPP (V_{max}) is referred from the specification. The input inductor is assumed to be large enough. The duty cycle of Q_1 can be found by the voltage gain equation of boost converter under continuous conducted mode (CCM) as follows:

$$D_{Q1\_Pmax} = \frac{V_{bus\_max} - V_{max}}{V_{bus\_max}} \tag{6}$$

Where V_{bus_max} is 80 V, V_{max} is 34.4 V and D_{Q1_pmax} is 56.8 %. After calculating D_{Q1_pmax}, the inductor is designed with a proper input current ripple at MPP ΔI_{L_pmax} by using (7).

$$L = \frac{V_{pmax} \times D_{Q1\_max}}{\Delta I_{L\_pmax} \times f_s} \tag{7}$$

Where ΔI_{L_pmax} is chosen as 28 % of the operating current at MPP (I_{pmax}). The inductance is designed 3 mH using (7). Although boost converter provides a continuous input current, there is still a small current ripple. Therefore, an input capacitor acting as an input filter is necessary. It improves the high frequency switching noise which may affect the I-V curve measurement. A larger capacitor leads a small input voltage ripple. However, it may also cause longer response time, extra cost and layout space. Filter capacitor C_{in} is calculated as,

$$C_{in} = \frac{\Delta I_{L\_pmax}}{8 \times \Delta V_{in\_pmax} \times f_s} \tag{8}$$

Where ΔV_{in_pmax} is the input voltage ripple at MPP, ΔV_{in_pmax} is chosen as 0.15 % of V_{pmax}, and the input capacitor C_{in} is calculated as 150 μF. C_{out} needs to meet the bus voltage ripple ΔV_{bus_pmax} at MPP. The output capacitor is designed by (9).

$$C_{out} = \frac{I_{bus\_max} \times D_{Q1\_pmax}}{\Delta V_{bus\_pmax} \times f_s} \tag{9}$$

Where D_{Q1_pmax} is 56.8%, f_s is 50 kHz, ΔV_{bus_pmax} is chosen as 1 % of V_{bus_max} and C_{out} is 64 μF.

MOSFET and diode are selected with proper current and voltage ratings. When the improved boost converter V-I curve tracer traces I_{sc} point, the duty of Q_1 is equal to 100%. Therefore, the maximum current flowing through boost switch Q_1 is I_{sc}. When operating at MPP, V_{ds_max} of Q_1 is V_{bus_max}. As a result, Q_1 is chosen as 100V/5A MOSFET. For the diode, when operating at MPP, peak inverse voltage (PIV) of boost diode and the V_{ds_max} of load switch are V_{bus_max}. Also, for both of D and Q_2, the maximum current flowing through them is the maximum bus current I_{bus_max} [14].

$$I_{bus\_max} = \frac{V_{bus\_max}}{R_{load}} \quad (10)$$

I_{bus_max} is 1.5 A, diode is chosen as 100V/3A Schottky diode and load switch Q_2 is chosen as 100V/3A MOSFET.

3. Simulation results and Inference

The proposed curve tracer is simulated to prove its feasibility by PSpice software. In this section, I-V curve and P-V curve are measured not only under uniform irradiance but also under partial shading.

Case 1: Uniform insolation condition

The two PV panels are operating under full irradiance level, I_{sc1} = I_{sc2} = 2.55 A. The characteristics curves are shown in Figure 5. The maximum power (P_{max}= 74.26 W) occurs when V_{op}= 34.04 V.

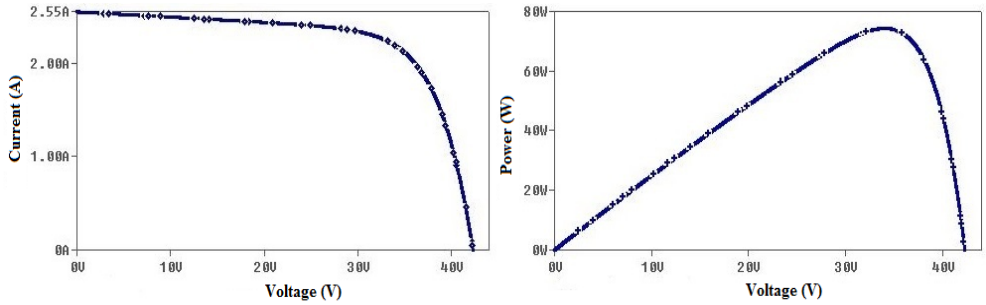


Figure 5. Characteristics of PV array under uniform insolation conditions (I_{sc1}=I_{sc2}=2.55 A)

Case 2: Non-uniform insolation condition 1

When PV panel operates under partial shading, I_{sc} value is reduced. Under different shaded levels, the global MPP may occur at higher or lower voltage as mentioned earlier. P-V curve has a global MPP at a lower voltage when $I_{sc2} < 0.5\ I_{sc1}$. A condition, I_{sc1} = 2 A and I_{sc2} = 0.7 A, is an example. The characteristics of this condition are shown in Figure 6. The global MPP of P_{max} = 26.41 W occurs at the lower voltage (V_{op} =16.25 V).

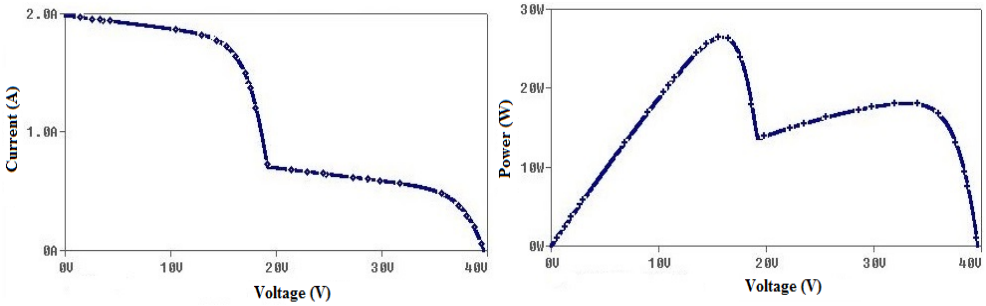


Figure 6. Characteristics of PV array under partial shaded conditions (I_{sc1}=2A & I_{sc2}=0.7A)

Case 3: Non-uniform insolation condition 2

On the contrary, the global MPP occurs at higher voltage when $I_{sc2} > 0.5\ I_{sc1}$. Under a condition, I_{sc1} = 2.55 A and I_{sc2} = 1.55 A, the characteristics are shown in Fig 7. The global MPP (P_{max} = 46.55 W) occurs at higher voltage (V_{op} = 34.86 V).

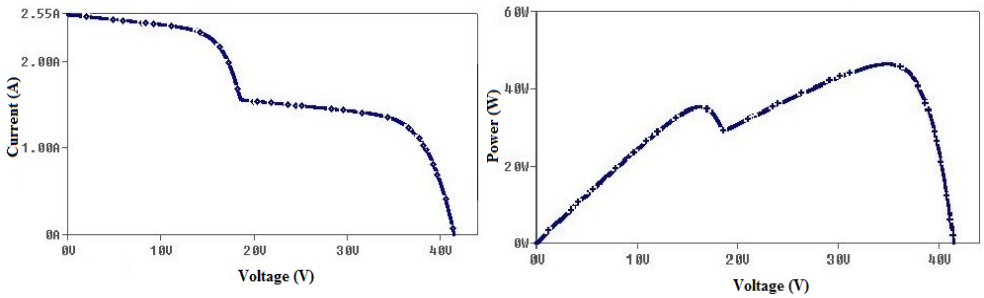


Figure 7. Characteristics of PV array under partial shaded conditions (I_{sc1}=2.55 A & I_{sc2} =1.55 A)

For different shading conditions, the developed tracing system is validated and results are consolidated in Table 1.

Table 1. Simulation Parameters

Insolation levels (W/m^2)	**Panel Currents (A)**		**Array Parameters**				
	I_{sc1} (A)	**I_{sc2} (A)**	**V_{oc} (V)**	**I_{sc} (A)**	**V_{max} (V)**	**I_{max} (A)**	**P_{max} (W)**
1000,1000	2.55	2.55	43.10	2.54	34.04	2.19	74.26
1000, 608	2.55	1.55	41.49	2.53	34.86	1.33	46.55
800, 275	2	0.7	40.20	1.98	16.25	1.62	26.41

4. Hardware Implementation

The proposed curve tracer shown in Figure1 is implemented in hardware with designed values. In this work two series connected panels are used for testing. One of the solar panels is kept under full illumination whereas another is subjected to partially shaded conditions, using artificial light source, as shown in Figure 8. In case of partially illuminated panel, the insolation level received by the module has been changed using tilting stand arrangement.

The improved boost converter is realized with proper component selection as discussed in Section 2. The switch used is IRFP460 (Metal Oxide Semiconductor Field Effect Transistor) which is TO-247 package type. It is an N-channel MOSFET and its rating is 500V and 20A. The diode used id IN5408 with the current rating of 3A. The inductor (3mH) is designed by winding appropriate turns of insulated copper coil on an E core. The hysteretic self-controlled DMLR circuit is simple and easy to be accomplished by applying a comparator µA741 with a positive feedback loop. µA741 is supplied by 15 V and a reference voltage is 5 V. The complete system is fed by the small PV array. The hardware setup of the power circuit is shown in the Figure 8.

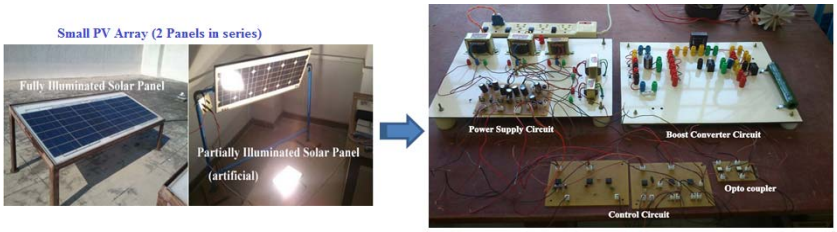
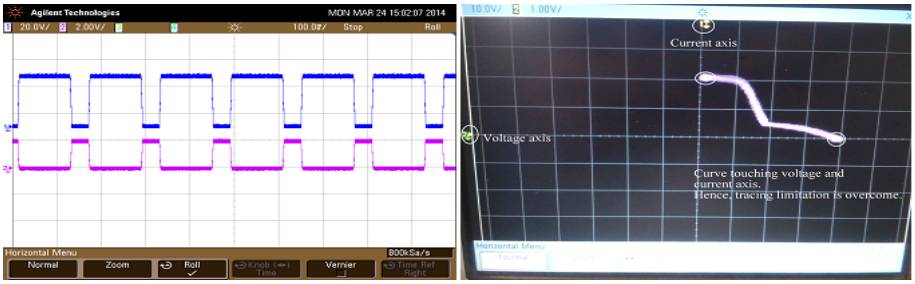


Figure 8. Hardware setup of the proposed curve tracer system

V_{op} and I_{op} of a PV panel are traced under partial shaded condition as shown in Figure 9.a. The oscilloscope is switched to X-Y mode to trace I-V curve, and is shown in Figure 9.b.



(a) (b)

Figure 9. (a). V_{op} and I_{op} of the panel under non-uniform irradiance. (b). I-V curve of the panel under non-uniform irradiance condition

The observed values are given below:
For panel 1 (fully Illuminated panel), V_{oc}= 20.7 V; I_{sc}=2 A.
For panel 2 (partially Illuminated panel), V_{oc}= 18.4 V; I_{sc}= 0.8 A.
For the small array (panel 1 and panel 2 connected in series), V_{oc}= 39.8 V; I_{sc} =2.1 A.

From Figure 9 (b), it is observed that the proposed curve tracer has no limitation near V_{oc} as well I_{sc} points. To check the proposed curve tracer, the various shading profiles have been introduced and the curves are traced. Figure 10 shows the tracing output for a case where panel 1 is illuminated such that it produces I_{sc}= 1 A and panel 2 is shaded such that it produces I_{sc}= 0.35 A. It is observed that this tracer has no limitation near I_{sc} and V_{oc} points.

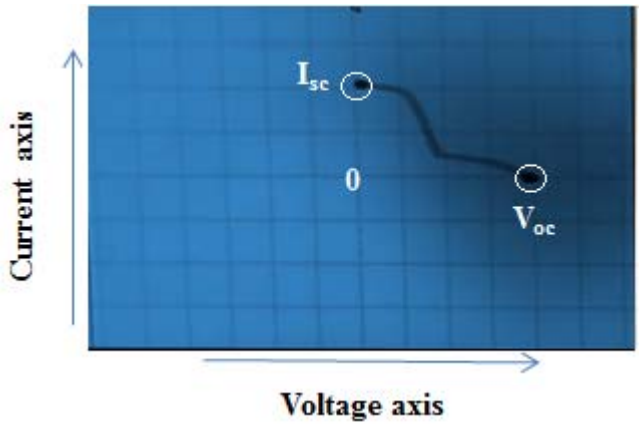


Figure 10. I-V curve of the panel under non-uniform irradiance condition (Panel 1: I_{sc} =1A, Panel 2: I_{sc} = 0.35 A)

5. Conclusion

In this paper, a load self-adaptive PV panel characteristic curve tracer has been proposed by applying a hysteretic self-controlled DMLR to a boost curve tracer. It has several advantages include its simple structure, cost-efficient implementation, and no tracing limitations near the V_{oc} area. The DMLR modulates its equivalent resistance from the rated resistance to infinite impedance by adjusting the duty cycle. The DMLR creates a new load line and ensures that the load operating voltage V_{bus} is always higher than the panel operating voltage V_{op}, thereby ensuring that the boost converter maps all panel operating points to load operating points using a constant power locus mapping technique. Consequently, the proposed curve tracer has no tracing limitation near the V_{oc} area. A 72 W PV panel prototype is simulated and implemented to verify the feasibility of the proposed curve tracer under partial shaded condition.

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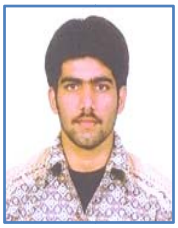

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