Low Power Designs of Current Steered DACs in CMOS Process: A Review

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Abstract: Low power design has become popular nowadays because ofdevelopment of improveddata converters with high resolution in CMOS process. Electronic device manufacturersare competing each other to produce devices that can extend battery life, have inexpensive packaging and cooling systems as well as reduce the size.The objective of this paper is to review various low power designs in digital to analog converters (DAC). The methods used to reduce the power consumption are presented in details. We focused the designs in the segmentation current steering DACs, as most of the low power designs illustarted in literatures are based on this architecture. From this review, we find that triple segmented architectureand spike free switching can reduce the power consumption effectively. This review paper can be a reference for the researchers and engineers to develop low power CMOS DACsfor various applications.

Keywords: Digital to analog converter, low power, segmentation, current steering, CMOS

1. Introduction

The rapid advancement in downscaling CMOS technologies, drive the devicesto portable, small size, high speed and consume low power [1-3]. Digital to Analog Converter (DAC), which converts the digital data to analog signal, has enormous applications in modern days. The digital signal is binary while analog signal is in forms of voltage and current. Digital to analog converter is commonly used inradio frquency identification (RFID) systems, signal processing, embedded application, industrial control systems such as in valves and waveform function generator. In television and mobile phone, the digital signal is converted to analog signal in sounds and images for human to recognize [4-9]. For embedded application, itis now used in medical applications for bio-implantable systems.

There are various types of DACs with their own advantages and disadvantages. The application of a DAC mainly depends on itsperformance parameters such as speed, output range, power supply requirement, resolutionetc. [10]. The operation of existing DACsare based on power width modulator (pwm), sigma delta, binary weighted, R2R ladder, thermometer coded, cyclic DAC and hybrid DAC. Low power design of circuitsare very important to extend the battery life, having inexpensive packaging and cooling systems as well as reduce the size.

The objective of this paper is to survey the low power designs of CMOS DAC for RF applications. Basically, there are three modes of circuit technology; voltage-mode, current-mode, and charge-redistribution mode, although charge-redistribution can be considered as voltage-mode as well. In a voltagemodeDAC, the element values (and the signal carrier) are given by voltage levelsas for example in a resistor-string that divides a voltage reference into a number different voltage levels. Withcurrent-mode, the DAC elements (and the signal carrier) be given bycurrents, as for example switched current sources or resistors dividing a major current intoweighted subcurrents. Finally, in charge-redistribution the DAC elements are givenby capacitor values, and the operation of the DAC is given by a switched-capacitor technique(SC). Since the focus is set on high-speed applications, the current-mode DACs gets muchattention to the researchers [11].

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Most DAC designs utilizing current steering architecture to achieve high resolution and high speed with low power consumption [12-13].Binary weighted current cell or unary decoded are steered to DAC output. This operation is relying on digital input code [14]. Its advantage is to drive resistive load without requirement of buffer. This make current steering as a suitable architecture for device requiring high resolution and high speed. Its ability is contributing by an array of matched current sources. [15]

Several architectures in the current steering are two stage, interpolatedand segmentation[16]-[18]. Interpolating DACs use a pulse density conversion technique that allows for the use of a lower resolution DAC internally. The drawback of this architecture is high circuit complexity, large power consumption and low conversion data rate and therefore, used in very limited applications. On the other hand, segmentation is widely used for signal processing application because of its ability to reduce the area and simplify the decoding logic complexity. Segmentation is weighting the least significant bit (LSB) in unary sequences and most significant bit (MSB) in binary sequences. The common DAC is consisting both of these sequences or either of them. The advantageous in binary sequence is the area but it needs large margin in chip fabrication and least accuray.

In unary sequences, it needs large area because of decoder consists of thermometer code. Larger die size is required and the layout becomes complicated. The conversion speed too becomes lower because of number of switches increases as 2^n. Meanwhile it's advantageous is accuracy as variation between the bits are constant. Thus, in segmentation the advantageous in both sequences are combined to get better performance in speed, area and low power. The advantageous of binary and unary sequence are summarized in Table 1.

Table 1. Comparison between unary and binary

Binary	**Unary**
Small area	Larger die size
High speed	Conversion speed become lower
Low accuracy	High accuracy

The trend in lower the power consumption has been given full attention in technology nowadays. From Figure 1, we can see that the power dissipation has decreased over time. However there are trade off between the power, speed and area. The circuit design will not exactly to have low power consumption with high speed and small area at the same time. Two devices with same resolution and technology will have different power consumption and area. In segmentation, when we want to implement the MSB and LSB part, we need to consider the static and dynamic performance along with how complicated it will be implemented. So, it will involve trade off between them.

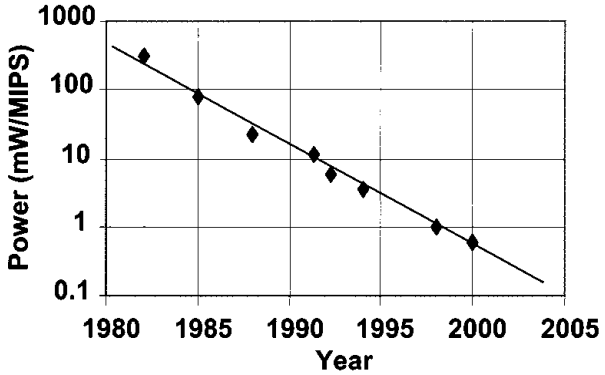

Figure 1. Power dissipation over time

When the size and density of chips as well as the systems are increasing, the important to provide adequate cooling will increase the systems cost and limit its functions. Techniques to reduce the power consumption of a design are therefore receiving more attention. The popularity of portable applications that prefer low power consumption to extend the battery lifetime, has added intensity to this quest. Examples of this can be found in the worlds of audio, video, and laptop computing.

2. Power Consumption In Cmos

Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching, and static power is consumed regardless of transistor switching. Dynamic power consumption was previously (at 0.18µ technology and above) the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. However, as the feature size shrinks, e.g., to 0.09µ and 0.065µ, static power has become a great challenge for current and future technologies. The dynamic power cannot be eliminated completely, because it is caused by the computing activity and it is still the major contributor to power consumption in CMOS circuits[19].

Power dissipation in a DAC is determined by the output impedance and drive-strength rather than architecture.Power in CMOS circuits is mainly consumed during the switching of the gates. Computing the dissipation of a complex gate is complicated by the $f_{0\to1}$ factor, with $f_{0\to1}$ the frequency of energy-consuming transitions (or $0 \to 1$ transitions for static CMOS) also called the switching activity.One concern is that the switching activity of a network is a function of the nature and the statistic of the input signals: If the input signals remain unchanged, no switching happens, and the dynamic power consumption is zero. On the other hand, rapidly changing signals provoke plenty of switching and hence dissipation. Other factors influencing the activity are the circuit style, the function to be implemented, and the overall network topology. The expression for the power consumption is

$$P_{dyn}=C_L\ V_{DD}^2\ f_{0\to1}\ =\ C_L V_{DD}^2 P_{0\to1} f \qquad (1)$$

where

C_L = Load capacitance

In this paper, different topologies in low power DAC circuits will be reviewed. Methods to reduce the power consumption as well as various technologies which have been developed and utilized to enhance the performance of DAC will be discussed in details.

Basic DAC Architecture

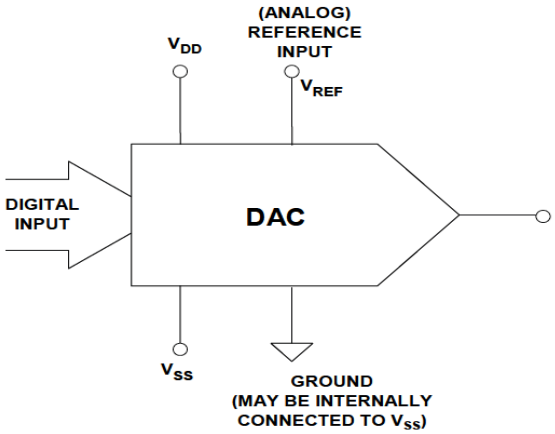

Figure 2. Basic DAC Architecture

3. Segmentation Current Steering DAC

Most of the low power designs of DAC utilizing current steering architecture. The segmentation DAC is chosen because of its high speed operation and high resolution. But, they experiencethe process variation, current source mismatch, and sycronizationof digital signals[20]. Current-steering DAC can be implemented with MOS-only components. Resistor-string or R–2R ladders are also very fast, but they require high-accuracy on-chip resistors. We will review the segmented consist of binary weighted and unary.

Figure 3 shows a basic configuration of segmented DAC. The paper describes a 10bit DAC[21]. They are two technique used in this paper to reduce the integral linearity error (INL) and differential linearity error (DNL). INL is caused by error distributions of current sources while DNL caused by an off-axis drain-source implantation. The techniques are hierarchical symmetrical switching and the layout technique of current sources.

This paper introduced a new switching method based on hierarchical error cancellationfor INL and a layout technique which suppresses the differential linearity error in DNL. The purpose of hierarchical symmetrical switching is to cancel the error distribution in INL by symmetrical switching. The graded and symmetrical errors are suppressed by this symmetrical switching method. For the new layout technique, the transistor is separated into two mirrored sub transistors joined in parallel. The sum of drain currents from both mirrored subtranstistor contributing to the output of current source. This design too can decrease the parasitic capacitance.This architecture used current cell matrix. The 7 MSB are segmented to non-weighted current sources and the 3bit produced by weighted current sources. In this paper, PMOS is used in the current sources to get the output swing easily and have less drain current.

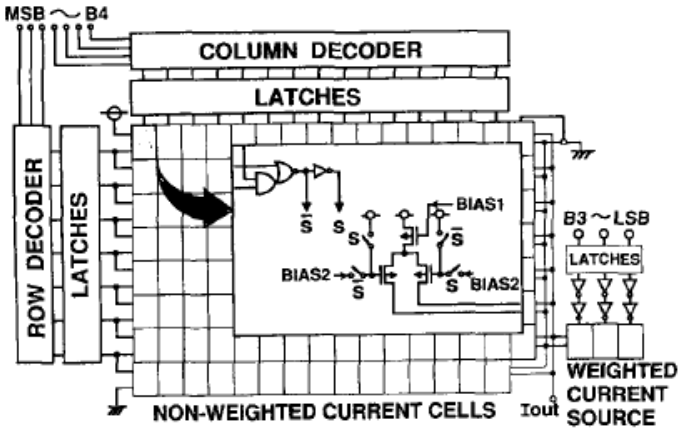

Figure 3. Segmentation DAC

The disadvantage of this design is it has high power consumption which is 170mW and requires large area. The active area is 1.56mm^2 while the chip size is 2.02mm x 1.87mm. However it contributes as a basic design to low power designs DAC later.

A10bit DACcapable ofgetting small area and low power discussed in [22].This design is for cell-based IC. To minimize power dissipation and area of current cell, it presented a method which considers the process difference.

Three configurations were considered by the author, they are switched capacitor, resistor string, and current cell [23-24]. Switched capacitor has high noise and resistor string is not easy to get low power and small area by just optimize the trade off. The advantage of current cell is, it has low impedance. This will make the design as the best choice for noise immunity.

The method used in this design is by reducing the gate area S_g, defined as WxL, given the allowable current error, the cell current Io, and relative errors, such as ΔVth, ΔW and ΔL. From the equation (1.1) we can get which parameter reduce the S_g.

$$S_g = W_{min}\ L_{min} = \frac{4\Delta W \Delta L\left\{\left(\frac{\Delta W}{\Delta L}\right) + Ar^2\right\}}{ArK\beta^2} \quad (2)$$

where

K_β = component caused by process variation
Ar = aspect ratio of the MOS transistor (W/L)

To ease the calculation, ΔW=Δ L in Equation (1.1) resulting$S_g$is minimum when Ar=1. Another method is to reduce the current cell sufficiently during fabrication. The disadvantage of this design is cell current value is suppressed among current cells. Large current error produced when effective gate voltage $(V_{gs} - V_{th})$is reduced. Figure 4 shows the configuration of DAC.

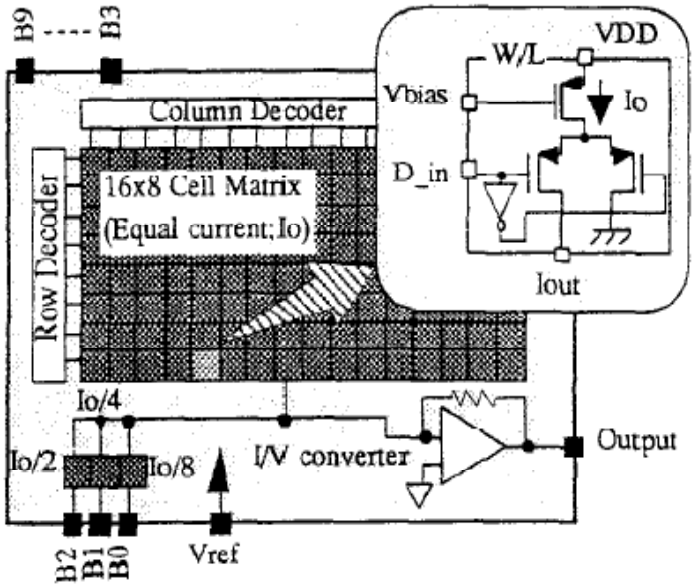

Figure 4. DAC Configuration

The purpose of the design in [25]is to get low power consumption with small area and enhance the linearity. This paper used triple segmented combining matrix array-arrays of current sources and binary weighted.Sample-to-sample variations and temperature drifts produce full scale errors. So, a gain error compensating circuit is used to amendthe full-scale errors. This design too, proved that the segmentation can be utilized in moveable communication product for intermediate operation range.

Note that this configuration is same as [21] but has triple segmented in order to get low power consumption. It consists of 10 bit D/A conversion cell, a biasing generator circuit, an internal output resistor R_L and an internal biasing resistor R_B. Switching technique in [21] ispresented to enhance the linearity and lower the parameter difference.

10bit DAC with segmentation architecture is implemented in [26]. This design has same number for binary and unary bit which 5 bit is for MSB and 5 bit is LSB. This design is actually for high speed DAC because it can achieve 1GS/s Nyquist frequency. The high speed is achieved by technique implemented in decoder and switch driver. To reduce the area, the layout parasitic effect and the architecture of the design is studied. This design has power consumption with 110mW at 1 GHz clock has small area of 0.35mm^2.Even though this circuit is successful to achieve a very high speed design but total power consumption is not relatively low which 110mW. However, the power consumption in digital part is just 6.2mW. Figure 5

shows the configuration of segmented DAC consists of thermometer decoder, switching matrix, dummy decoder, clock and latch.

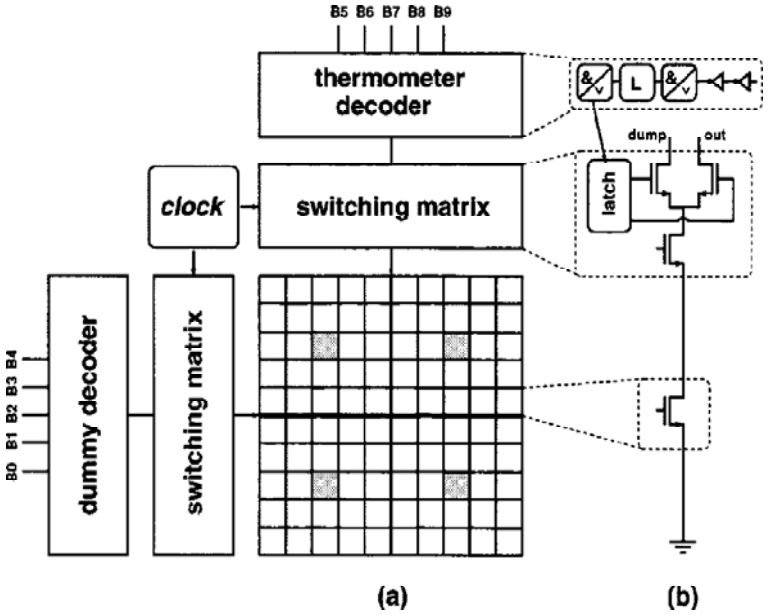

Figure 5. DAC Configuration

A low power DAC for portable electronic is design in this paper [27]. To achieve low power consumption a current mirror with spike-free switching is presented. On the other hand, this current mirror too can improve the INL and DNL.Differential switch pair is used in current switch. To make MOS in operation, dummy load is put at difference side of differential switch. However, more power is consumed when the dummy load is put at difference side.

This design used a technique call spike-free switching implemented in current cell. Current cell output voltage is on fixed voltage level when current cell is off. This will prevent power dissipated in dummy load. Moreover, this design not implement any deglitch circuits. This leads to low power and does not use many components. This DAC consumes power at 2.5mW at voltage supply of 1.8V.

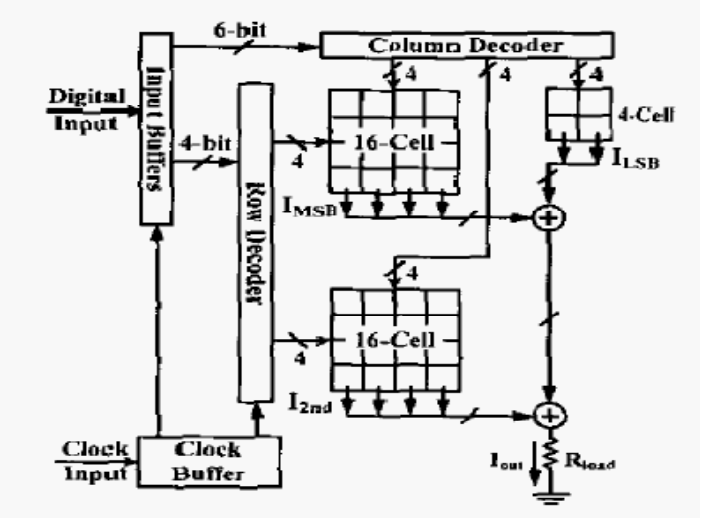

Figure 6. Two stage Configuration

Figure 6 shows the configuration of reviewed DAC. Current cell matrixes in three stages are suggested to keep the number of current cell minimum and simplify the column and row decoder. This is based on design proposed byKuo and Wu[28]

The advantage of this design is it didn't have dummy load but changed with reference voltage, V_b. As discussed above, a spike free switching is introduce in Figure 7 to get low power consumption and turn-on time mechanism when needed. Reference voltage is used to steady the voltage oscillation.

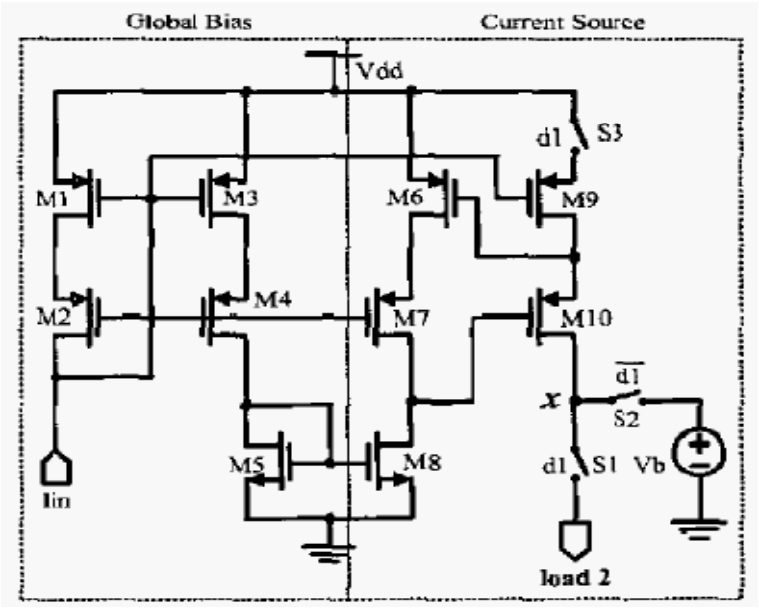

Figure 7. Proposed spike-free current current mirror

In [23], the design has been proposed that has 14 bit resolution with low power consumption. To reduce the power consumption, a mixed voltage process method is used. The supply range is from 1.7V – 3.6V. Analog section will operate from higher voltage supply compared to digital section in mixed voltage process. This will make the output voltage compliance and swing will be larger.

Fundamental structure is shown in Figure 8. They are three categories in current supply for current steering. First categories is from digital and clock part and straight scales with data activity and sample frequency. The analog from full scale output current is in second and third categories. Finally, comes from bias circuits and bandgap reference. The advantage is, process and supply voltage scaling improvement can affect the power consumed in CMOS.

In this paper, several circuit techniques are introduced which producedlarger output signal equivalent with AC distortion performance with power dissipation 10 times larger. One of them is the switch driver bias circuit shown in Figure 9. This design can be interfaced with different parts of signal series which need the output voltage of 1.2V with voltage supply of 3.3V. However, the disadvantage is current flows through output ignoring the applied digital input because of every current source is on.

Three major functional blocks are CMOS decode logic/clock/switch drivers, output current source array and analog bias blocks with band gap reference. Power consume in this design is 0.28mW for 3.3V supply voltage and 0.17mW for 1.8V supply voltage.

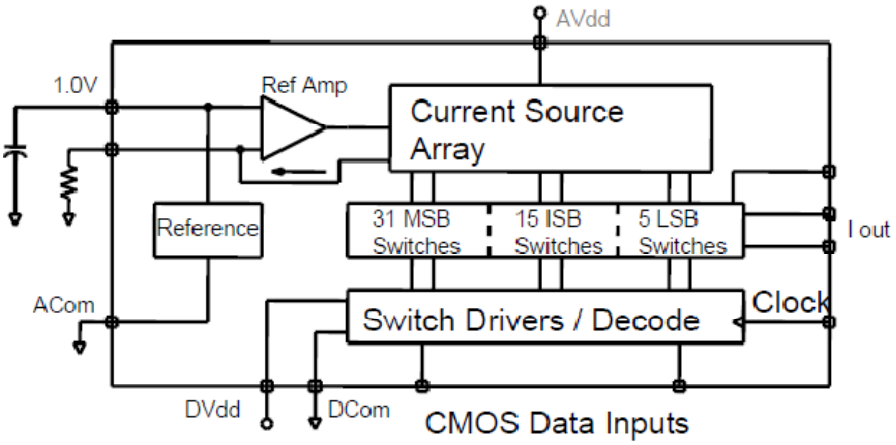

Figure 8. DAC Configuration

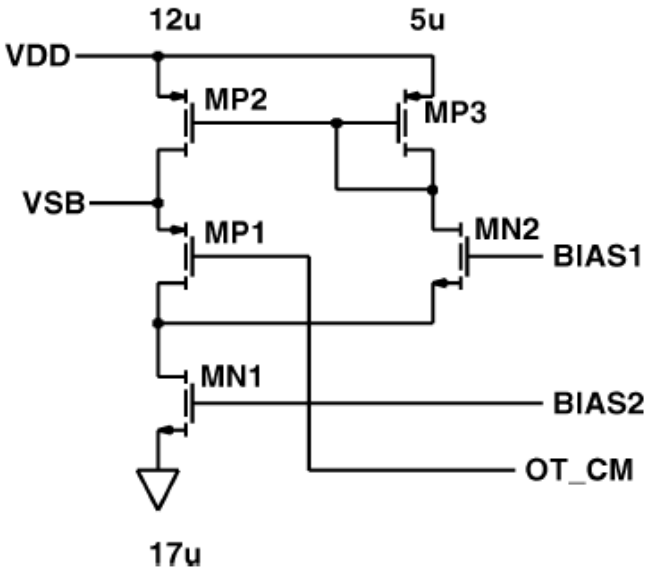

Figure 9. Switch driver bias circuit

The purpose of [29] is to designa 6 bit DAC toget a small die areawith low power consumption. The design is used for WPAN transceivers.To enhance the dynamic performance,regulated cascode current sources and master-slave deglitch circuit are suggested.Deglitch circuit influences the rising and falling time of output signal.To minimize power and area, the function of deglitch is integrated inside edge triggered flip flop.

Glitch noise is caused by data skew and impedance lowering. It is important to minimize them because glitch is one of the sources in power consumption. A master slave deglitch circuit is suggested together with optimizing the current source switch size to decrease the data skew. Moreover by using this circuit, dynamic performance will be improved because glitch will degrade the dynamic performance.

Gate capacitances must be equal for every switches to reduce the difference slew rate and delay. W/L ratio is getting by switching current. To obtain the equal gate capacitance the switch size is made by controlling the length and width. To design the width and length, Equation of (3) is used which is from Equation (4) and (5).

$$C_{OX}(W_{MB}L_{SB}) = C_{OX}(W_{LSB}L_{SB}) \quad (3)$$

$$L_{SB} = \sqrt{L_{MSB}^2 \times 2^{I_{MSB}/I_{LSB}}} \quad (4)$$

$$W_{LSB} = \sqrt{W_{MSB}^2 \times 2^{-(I_{MSB}/I_{LSB})}} \quad (5)$$

Power consumption and area are connected to the segmentation. This is because number of logic gates to control the current sources is correlated to the segmentation. Furthermore, the linearity is also connected to segmentation.

Figure 10 shows the connectivity on the number of binary weighted bits for the segmented 6bit DAC. Hardware complexity decrease when binary bits increase but the linearity becoming bad. Therefore, when decide on segmentation, trade off between hardware complexity and linearity is needed.

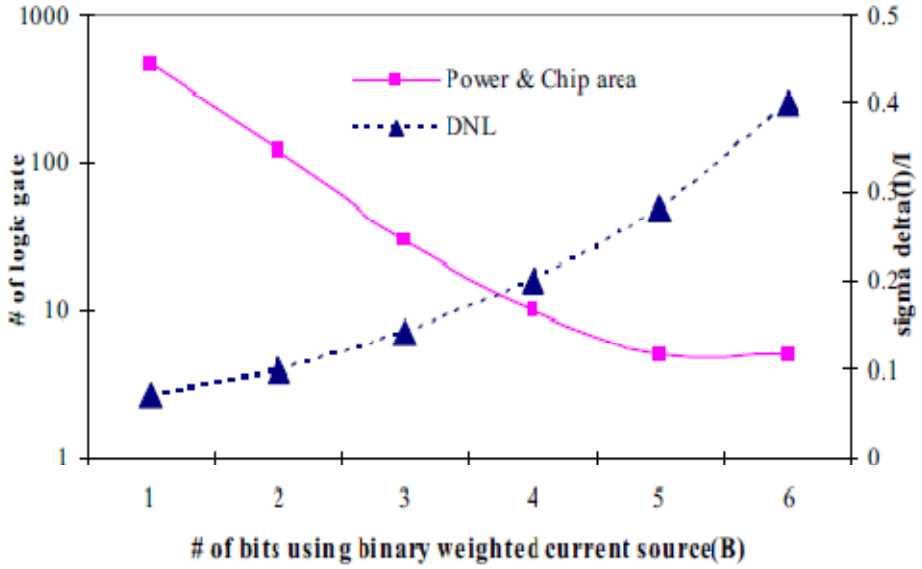

Figure 10. Relation of power and area to number of bits

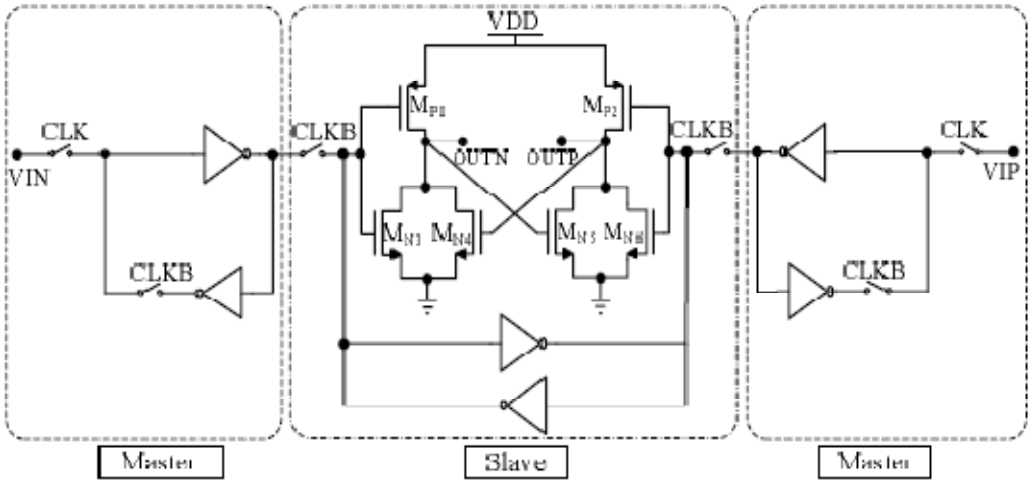

Figure 11. Master deglitch circuit

Differential output signal can be lowered when deglitch circuit controls the rising and falling time ofthe output signal. To minimize the power and area, a method is used by connecting the deglitch function inside the edge-triggered flip-flop, to get synchronization.Deglitch circuit method too has been implemented in [26]. Figure 11 shown the proposed master deglitch circuit.

In [30], the paper proposed 8 bit DAC which the aim is to obtain optimal performance with small area. The circuit is implemented into 6 MSB and 2 LSB sequences. Problems in latch-up, matching, and gradient induced error are look out by various techniques. To improve DNL and INL, current sources in current matrix need good matching. Layout structures called interdigited commoncentroid layout have been introduced for current matrix to give good matching. Physical and electrical properties of current cells differ through the gradients of matrix. The INL performance is affected by the gradient errors. The arrangement of the rows and columns has been put in random order, as shown in Figure 12.

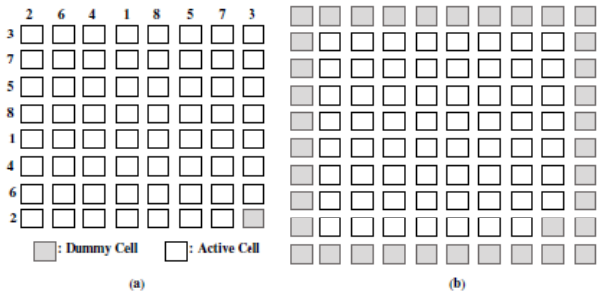

Figure 12. Randomization of the unit current cell matrix and the use of dummies

Latch up can happen in CMOS circuit. Some remedial protections are utilized in DAC layout to avoid latch up. Of them is kept NMOS and PMOS layoutspacing larger than minimum gap. When spacing are kept larger, minority carrier injection can be reduce and assisting to avoid latch up [31].

Larger transistors can enhance the unit current cell- transconductance gm of current source. However, parasitic capacitance will enlarge at the output node caused reducing the bandwidth of current cell and low frequency pole. Trade-off between the output impedance and the bandwidth of the current source will give the best possible size of transistors.

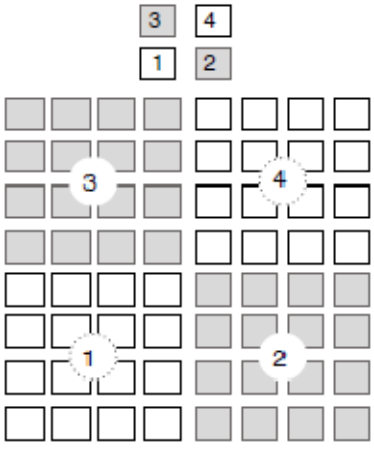

Figure 13. Biasing sceme of the MSB current cell matrix

The configuration of the unit current cell matrix of the MSB unary architecture is shown in Figure 13. Unit current cell matrix is separatedto four quadrants. Everyquadranthas 16 unit current cells and one current cell is unused in quadrant 2. To enhance DNL and INL, dividing the biasing of the main matrix into four quadrants is utilized. This DAC will be used in wireless telecommunication applications and the simulation shows this DAC consumes power consumption at 7.88 mW.

In [32], proposed design combines three differentarchitectures to achieve low power and low area.It was observed that a trade-off exists between the area occupied by the design and the error associated with the linearity of the DAC.The disadvantage of this designs is some compromise had to be doneregarding INL and DNL because value are too high. Even though the author claim this design can reduce area, the circuit is too complexbecause three different architectures are combine which are symmetric current cell matrix,binary divided current cell, and binary weighted current cell. This circuit too has just moderate accuracy. The circuit implemented two-stage design matrix by Kim and Yoon to minimize the number of unit current sources required to build the thermometer decoded [33].

The advantage of this design is it uses 1.2 V as supply voltage. This meets the requirement of reducing power. The second requirement is met by using minimum transistors as possible to implement the design. However, in the design, minimum transistors are dominantin reducing the power than low supply voltage. The power consumption of this design is only 1.443mW.

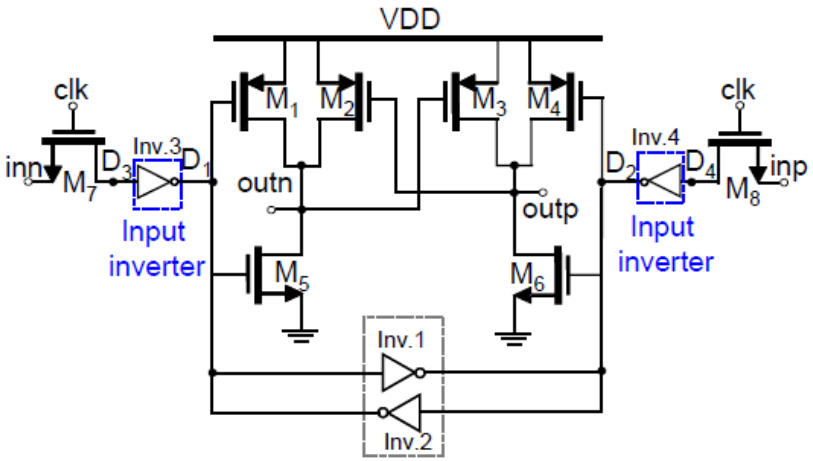

Figure14. Deglitch latch

In [33], 5 bit current steering DAC with low power is presented for UWB transceivers. The segmented structure choose in this design is to balance between the DNL error and complexity of the circuit. A bipolar current source cell consists of both PMOS and NMOS transistors are employed to save the power consumption compared to other designs discussed which used NMOS or PMOS. In the design, the current source sizing and INL yield are two parameters that are important. Moreover, for synchronization of the control signals at the switch transistors, a de-glitch latch is utilized to decrease the clock feed through from the pass transistors[26], [35]. The Figure 14 shown is the deglitch circuit proposed.

Reconstruction filter is used to form the spectrum in wideband wireless communication systems. The high conversion rate is desired to ease the requirement of the filter. System clock is designed at 1.35 GHz to balance the complexity of the filter and power consumption. At maximum conversion of 1.5 GSPS, the DAC consumes 10.4mW.

In [34],a small area and low power consumption current steering DAC with good linearity is suggested.Partially segmented DAC architecture is used to obtain these objectives. To achieve good linearity, common centroid layout and deglitch circuit are implemented in the current cell [26], [33], [35].The design is for UWB communication system and need towork in

GHz sampling frequency range with 8 to 10 bits resolution. Current mode is used because noise performances and speed are crucial thanthe range of output.

Technique of combining binary weighting for LSB together with segmentation in MSB is a good arrangement way between accuracy, dynamic performance, power consumption and chip size. Fully segmented is for Upper 6 bits and lower 4 bits are for binary weighted. 6 MSBs are separated into 2 groups and decoded by row and column decoders. 3 binary MSBs are converted to 7 thermometer codes by binary to thermometer decoders. Matrix cell decode is controlled by column thermometer codes and decoded row.

Timing mismatches between current reference switch controlling signals can produce glitch in output voltage. To prevent both two switches in the current source closed simultaneously, deglitch circuit is used. Crossing point of those two signals can be controlled when using this circuit.Signals can cross at lower value and avoid glitches when PMOS switches are used.This DAC utilizing partially segmented architecture consumes only 49.5mW with active chip areas is 2.2l mm^2. The disadvantage of this design is that it has bigger area than previous discussed design. The power consumetoo is not relatively low.

In [36], a 10-bit is proposed a low power current steeringDAC. To reduce power consumption, a new method called 4-D matrix structure of thermometer decoding has been used. This method is effective to reduce the area of digital section and design complexity.

Figure 15 shows the multisegmented architecture of proposed design. The input 10-bit binary code is divided into twosmaller codes. For 2-bit LSB part, binary weighted strategy hasbeen used. The 8-bit MSB part uses thermometer decoding but instead of using one single decoder it uses four 2-to-3 binarytothermometer decoders that occupy smaller area than formersingle decoder strategy. It can be shown that in a binary-to-thermometer decoder βbits increase in the input binary code, increases complexity,the number of control signals and power consumption witha factor of 2β. The proposed DAC has the advantage of using anovel 4-D matrix structure instead of conventional row andcolumn decoding strategy which leads to considerable reduction in powerconsumption, effective area of digital section and complexityof the design. For example for a 10-bit D/A converter with9 bits using thermometer-coded and 1 bit binary weighted, hasonly 12 control signals. Another advantage of thisdesign is considerable reductionin the number of cells, 255 cells compared to 511 cells of 3-DDAC. Four-corner simulations have been carried out at 1.7 MHz and 99 MHz frequency and simulation results show that the 10-bit DAC operates with power consumption of 51 mW.

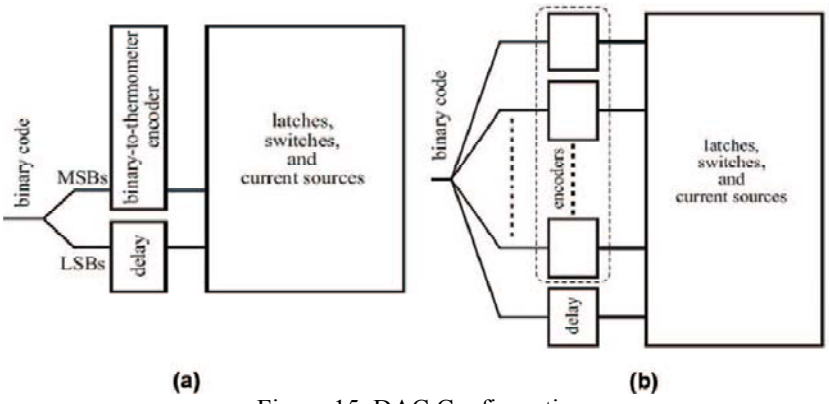

Figure 15. DAC Configuration

In[37]a 10bit DAC is presented. To produce low power consumption, two methods have been presented. First, is by switch driver power awareand second by a power optimized switch driver implementation. The first method is implemented in current cell. Moreover, routing related wiring capacitance is reduced by using a thermometer decoder whichreduces power consumption. The advantages of this design is, it is successful to achieve low power

consumption which is only 27mW when converting near Nyquist rate at 1GS/s compared to [26]and[34].

A 2-D INL bounded switching technique is presented in 6 bit DAC [38]. 2-D current mismatches and timing synchronization error are reduced by the suggested current cell switching technique in row and column lines. The suggested area efficient deglitching circuit requiresfewer transistors by 40% than the previousdeglitching circuits [34].To more improve the INL characteristic, INL bounded switching technique withgreatest static performance in 1-D switching schemesis enhanced and transform to the 2-D. Spurious-free dynamic range (SFDR) performance degraded by the output dependent delay andthe unsatisfactory synchronization of switch control signals.For clock synchronization and minimizing the timing error, a master-slave deglitching circuits aremostly applied[34-35]. This DAC consumes 11.9mW with low area of 0.11 $mm^2$and SFDR of 40.8dB. This design has smaller area and low power consumption with high conversion rate.

4-channel 8 bit DAC is proposed in [39]. To reduce power consumption and for embedded application, filter called two-times interpolation filter with 4 channels' parallel inputs is attached to the DAC input. Pre-filtered high frequency distortions and improved sampling speed are determined by the interpolating filter. It is also used to certify sufficient Signal noise Ratio (SNR) of digital input. When embedded in the System on chip (SoC), this filter is build to the front of DAC as the link between DAC and digital baseband. In addition to that, double centroid current array layout is utilized to prevent systemic and graded errors. The advantage is the small area with just $0.66\,mm^2$. However this designed consumed power at 18mW at 650MS/s sample rate.

8 LSB and current cell 4 MSB segmentation is proposed in[40] to reduce die area and optimal operationof binary weighted current. The advantage of this design is, fully differential amplifier is used to reduce harmonic distortion, operate at low supply voltage and give differential voltage output.The scaled current is moved from the resistor ladder output into differential voltage output by FDA. To make the voltage level efficient,low pass filter is used to filter out noise at high frequency in other design.It is important in establish the operation of DAC such as its lenience to device parameter variation affected by the supply voltage, environmental temperature, and others. Bad synchronization of control signals caused the DAC dynamic performance to degrade. To overcome this problem, latches are used between current switches and control signals. This will make control signals turn up at the switches at the same time. This design is able to operate at 0.72V and the first design working at very low supply voltage. This design will be applied in a bio implantable system for medical applications.

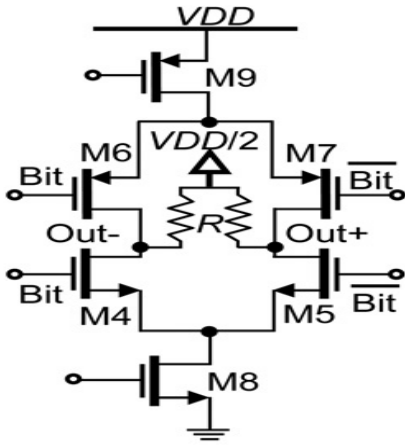

Figure 16. Bipolar current sources

In [41], a 6 bit segmented architecture combined withthe pseudo-thermometer structure is proposedto achieve a balance between the operating speed of the decoder andthe current source

cell's area. Furthermore, the presented pseudo-thermometer structure enhances the DAC's dynamic performance. The bipolarcurrent source cell and latch clock delay technique areadopted to reduce the power consumption [25]. A compactlayout is also accomplished by employing the proposedcompact de-glitch latch and the simple centroid switchingscheme. The compact de-glitch latch presented in this study simplifies the conventional latch design and layout in [42]. Furthermore, this latch brings another advantage of reducing the capacitance after the pass transistors, and thus the required input signal strength to cut the power of the input buffers is reduced. The active area is just 0.0585mm^2 with 5.4mW power consumption. Figure 16 shows the bipolar current sources.

In [43], the author proposed switching technique and current cell design which can minimize the power consumption in 12 bit DAC. Switch is turned on by latch and signal in the next cell is activated. Latch controlls the switch and source. Considerably amount of decreasing power consumption has been obtained when process of switch-on operate in individual.By implementing the sequential switch-on process in source similar with thermometer decoding, power can be reduced.

Increasing the number of bits produce a large amount of power consumed in cell array block.To overcome this problem, it is important to have cell operation that can minimize the power consumption. The advantage of this design is, the current cell has switch-on process when high state is selected by the matrix code in cell array. It is turned off when low logic state is selected. Compared to the normal differential switch and current cell source, every current sources are on state create current pass through to output without depending on the input. This process leads to increase the power consumption.In this design, it has achieved to reduce the power consumption 35% less than normal structure which is 14mW.

4. Discussion

Ohm's law (V=IR) describes the voltage output. Voltage output is related to current and load value. The die size and power dissipation will enhance when output current is increased. This is because to follow the reliability rules of electro migration. This rule indicates that increasing width of output and connection lines of each current source will increase the power dissipation and die size.By modify the output load value; output swing is amending to keep the similar cost and power. Thus, the current cells will operate within operating specification when the maximum range of voltage is not exceeded.

Circuit in [41] is similar with this design.In this suggested design, 3bit pseudo thermometer decoder used in [36] is utilized to enhance the dynamic performance and ease the current cell matching requirement for DNL given. To give enough output impedance and satisfy the static matching, current cell transistors must be designed appropriately.

$$(WL)_{min} = \frac{1}{2}\left[A_\beta^2 + \frac{4.A_{VT}^2}{(V_{GS}-V_T)^2}\right] / \frac{\sigma(I)^2}{I} \quad (6)$$

with $\frac{\sigma(I)^2}{I}$ as the relative LSB current source standard deviation. A_β and A_{VT} as the process parameters.

Switches that have minimum length can obtain low power consumption.Because of this, minimum lengths (W/L ratio of nMOS and pMOS) of switch transistors are designed as 0.3 μm/0.1 μm and 0.9 μm/0.1 μm.For easy realizing from the supply voltage, rail-to-rail switch control signals are applied. Master and slave latches are developed by the cascade latch as suggested in [36].

Furthermore, this cell will be used in rail-to-rail voltage-source applications and communication because cells DAC have high speed operation. Switching the cells and linking one of gain control resistors can enhance the step size of output voltage. It produces 8.32mW power consumption, with 6.4mV step size in 1.2V voltage supply.

The FOM is used to measure the performance of DACs as in Equation 1.6. Power, number of bits and sample rate are dependence to FOM. To compare designs that has been reviewed, these parameter will be given attention

$$\text{FOM} = \frac{\text{POWER}}{2^{\text{N}} \times \text{Sample rate}} \quad (7)$$

Method	Supply Voltage	Power	Area	Frequency Or Sampling rate	Remarks
Triple Segmented [25]	1.2V	1.443 mW	Not mention	5 MHz	to improve the linearity while minimizing the circuit area and gain error by compensating circuitry employed to correct for full-scale errors
Spike free Switching [27]	1.8V	2.5 mW	0.27 mm^2	10 MHz	to improve the INL/DNL and reduce the power consumption of the high-speed current steering DAC
Deglitch Circuit [34]	1.8V	49.5 mW	2.21 mm^2	1.25 GHz	to exhibit good linearity
Bipolar current sources [43]	1.2V	5.4 mW	0.0585 mm^2	2.7 GHz	To improve the DAC's dynamic performance, and employing the bipolar current source cell and latch clock delay technique reduce the power consumption in the analogue and digital parts

From the table provided, parameters involved in DAC are given. They are technology used, layer, resolution, DNL, INL, SFDR, sampling rate and voltage supply. From analysis, the lowest power consumption is 2.4mW in [25]. This design used triple segmented architecture to achieve low power consumption. The area of this design is relatively small which 0.45 mm^2 is. From the table, we can see that most of the design used 0.18μm technology with variety of layer. From the designs discussed above various methods to reduce the power consumption has been implemented. We found that authors of [26], [32], [35] have chosen deglitch circuit as a method to reduce the power consumption. From the table, designs with same resolution are compared. For 10 bit, the lowest power consumption is 2.4mW. While for 12 bit resolution design in [14] gets the lowest power consumption is 13.4mW. For 6 bit resolution, the lowest power consumption is achieved in [32] which is 1.443 mW. This design use triple segmented. From the table, designs in [24], [27], [41], [43] are the best designs with low power consumption and better performance compared to other designs. In addition to that, these designs too have advantage in smaller area. From Table 2, triple segmented and spike free switching contributed the lowest power consumption.

5. Conclusion

Various techniques to decrease the power consumption have been reviewed. One of the techniques to reduce the power consumption is to consider the process variation by reduce the size of current cell during fabrication. The second method is to implement triple segmented in the design. For low power consumption, spike-free switching isintroduced in the current cell.Another method to minimize the power consumption is by mixed voltage process. However, this method requires adding calibration circuit and noise splitter. This will make the circuit complex. Combining three different architectures and used of deglitch circuit too is one of the method used to reduce the power consumption. However, based from the analysis of all the parameters, designs using triple segmented and spike free switching have low power consumption compared to others. In the future, design of DAC by combining these techniques can be implemented to achieve better low power designs.

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