Toward CMOS Process-Compatible Gold Nanoparticles Deposition with Pattern for Electronics Application

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Abstract: Two approaches in nanoscale device fabrication are the top-down and bottom-up approach. The later method promises application in VLSI technology but a major challenge existed: integration for other devices as well as electrodes. Described in this paper, we have optimized preparation process for photoresist coating and photolithography. Patterned gold-nanoparticles has been successfully deposited on top of a silicon substrate using positive photoresist as a mask. SEM characterization confirmed the presence of nanoparticles with average diameter of 55 nm while as EDS spectrum confirms the presence of gold nanoparticles on the patterned Si substrate.

Keywords: Gold nanoparticles, CMOS-compatible, photoresist, patterned deposition.

1. Introduction

Electronics device miniaturization has brought many advances in devices performance, such as an increase in speed, packing density, lower power consumption as well as cheaper manufacturing cost [1, 2, 3]. Intel and ST Microelectronics has demonstrated MOSFET with 15 nm of gate length [4, 5]. However, further device scaling is facing its limits due to the fact that parasitic effect will become more dominant which leads to degradation in device performance [6, 7, 8].

Several studies have been conducted in the field of the nanomaterials-based device [9]. Cui et.all [10] has successfully made an attempt in fabricating Silicon Nanowire Field Effect Transistor (SiNW FET) with a bottom gate where they use a 5 nm silicon nanowire as a channel connecting source and drain. The nanowires were grown by nanocluster-assisted growth method, then deposited on top of oxide layer via ethanol suspension.

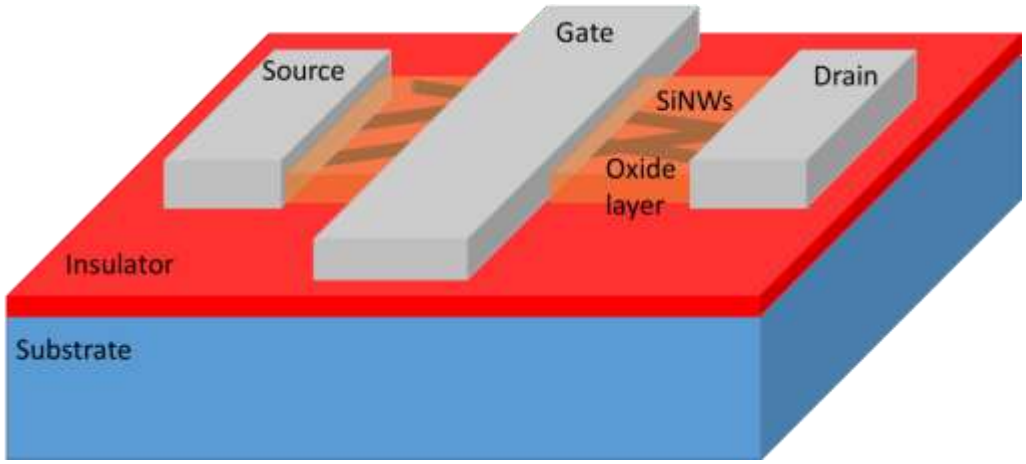

Figure 1. Schematic of a SiNW based FET

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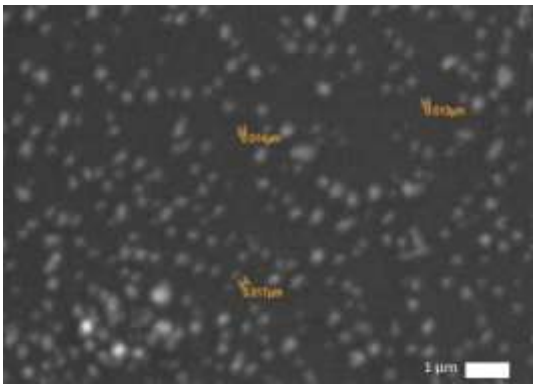
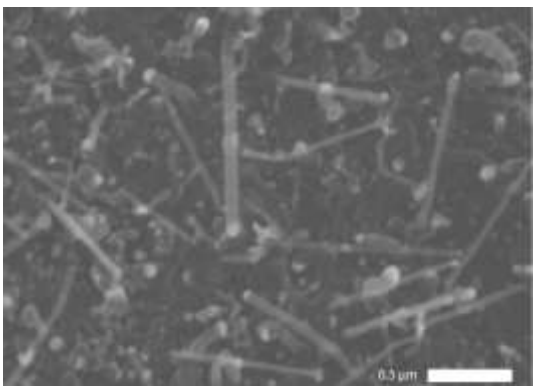
We plan to fabricate SiNW based FET using a top gate as shown schematically in Figure 1. We choose to use a top gate instead of a bottom gate to approach the conventional CMOS fabrication process. Also, using top gate will give a better performance like better subthreshold, higher transconductance and negligible hysteresis. Another advantage is that by using a top gate, SiNW surface will be covered by gate oxide preventing surface charge effect to influence the channel transconductance. As our first step in fabricating SiNW based CMOS, we begin by aligning SiNWs with metal contact by using patterned deposition of gold nanoparticles on top of the substrate. In this paper, we will discuss the patterned deposition of gold nanoparticles on top of a silicon substrate using conventional photolithography and dip coating method.

To extend the capability of device miniaturization, two common approaches are used, top-down and bottom-up approach. Top down approach is done by increasing the resolution of lithography in device fabrication. However, this approach will face constraints due to the limitations of lithography techniques which requires resolution to less than 5 nm, leads to very expensive cost [11]. To avoid the need for very high-resolution lithography in the fabrication of nano-sized structures, a technique to synthesize materials (nano-particle and nanowire) by so-called bottom-up approach is required.



(a)

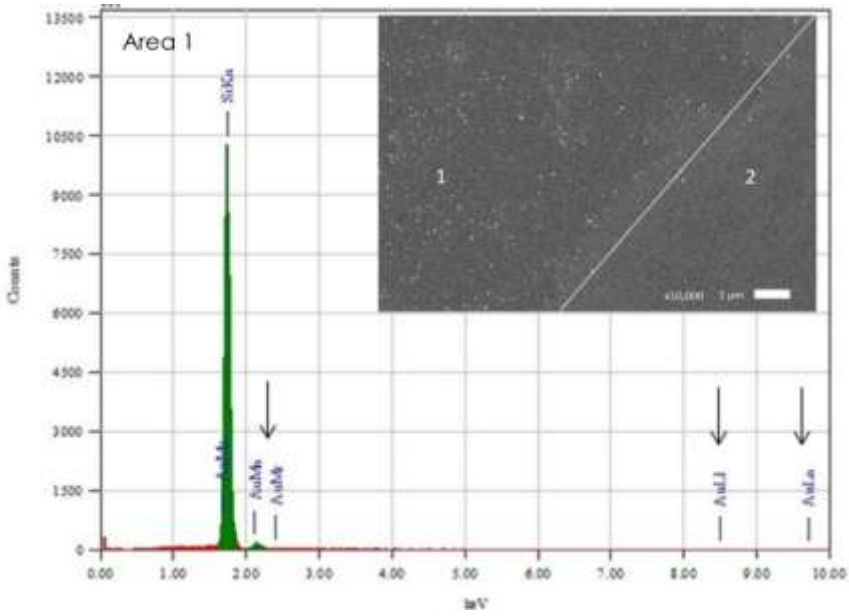


(b)

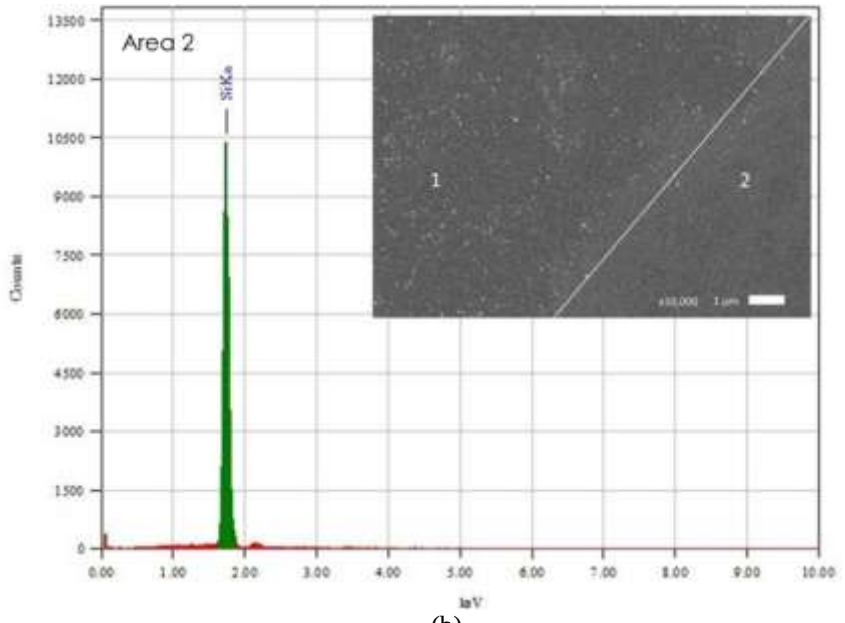
Figure 2. SEM images of the previous result: (a) Gold nanoparticles deposited on a silicon substrate and (b) Silicon nanowires are grown using the gold nanoparticles as catalyst.

To synthesize nanoparticles, various techniques have been developed: mechanical approach (e.g. particle milling) or chemical approach (egg. Turkevich method and Plasma Enhanced Chemical-Vapor-Deposition). In Turkevich method which we used in this study, high purity

Figure 3 shows the AuNPs deposited on the sample both on the area covered with photoresist and exposed area.



(a)



(b)

Figure 4. (a) EDS spectrum of area with AuNPs (b) EDS spectrum of area without AuNP.

Next experimental step is pattern development, which involves standard lithography process, from resist coating, pattern transfer via exposure and development. Silicon wafer is cleaned using standard RCA process and then coated with photoresist by spin-coating, and then baked at 80^{o}C for 3 minutes. Subsequently, the sample is baked at 120^{o}C for 8 minutes. We then proceed with dip coating process by immersing the sample in aqueous AuNPs solution for

distinctive between AuNp density in the coated and uncoated area. The difference is in a ratio of 1:9. Our simpler methods and promising results have paved away for our next goal which is to synthesize SiNWs using deposited AuNPs as catalyst to fabricate self-aligned SiNWs for SiNW based FET.

5. Acknowledgement

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6. References

[1]. Wong, Hon-Sum Philip, et al. "Nanoscale CMOS." *Proceedings of the IEEE 87.4* (1999): 537-570.

[2]. Yamauchi, Hiroyuki. "Embedded SRAM trend in nano-scale CMOS." Memory Technology, Design and Testing, 2007. MTDT 2007. *IEEE International Workshop on. IEEE*, 2007.

[3]. Jo, Sung Hyun, and Wei Lu. "CMOS compatible nanoscale nonvolatile resistance switching memory." *Nano letters 8.2* (2008): 392-397.

[4]. R. Chau, B. Doyle, M. Doczy, et al, "Silicon Nano-Transistor and Breaking the 10nm Physical Gate length Barrier", *Proc. of Device Research Conference 2003*, pp. 123-126. 2003.

[5]. F. Boeuf, T. Skotnicki, S. Monfray, et al., "16 nm Planar NMOSFET Manufacturable Within State Of The Art CMOS Process Thanks To Specific Design And Optimization", *Proc. of IEDM 2001*, pp. 29.5.1 - 29.5.4., 2001.

[6]. H.-S. P. Wong, "Beyond the Conventional Transistor", *IBM Journal of Research and Development*, Vol. 46, No. 2/3, pp. 133-168. 2002.

[7]. Taur, Yuan. "CMOS scaling beyond 0.1 μm: How far can it go?." VLSI Technology, Systems, and Applications, 1999. *International Symposium on. IEEE*, 1999.

[8]. Olson, Brian D., et al. "Simultaneous single event charge sharing and parasitic bipolar conduction in a highly-scaled SRAM design." *Nuclear Science, IEEE Transactions on 52.6* (2005): 2132-2136.

[9]. Schmidt, Volker, et al. "Realization of a Silicon Nanowire Vertical Surround-Gate Field-Effect Transistor." *Small 2.1* (2006): 85-88.

[10]. Cui, et.all. "High Performance Silicon Nanowire Field Effect Transistor". *Nano lett.*, Vol. 3, No.2 , pp. 149-152, 2003.

[11]. DRS Cumming, S Thoms, SP Beaumont, JMR Weaver, "Fabrication of 3 nm wires using 100 keV electron beam lithography and poly (methyl methacrylate) resist", *Applied physics letters 68 (3)*, 1996, 322-324.

[12]. Asep Rohiman, Isa Anshori, Akhmadi Surawijaya, Irman Idris. "Study of Colloidal Gold Synthesis Using Turkevich Method". *AIP Conf. Proc*. 1415, p. 39, 2011.

[13]. Kimling, J., et al. "Turkevich method for gold nanoparticle synthesis revisited." *The Journal of Physical Chemistry B* 110.32 (2006): 15700-15707.

[14]. Zhao, Pengxiang, Na Li, and Didier Astruc. "State of the art in gold nanoparticle synthesis." *Coordination Chemistry Reviews 257.3* (2013): 638-665.

[15]. R.S.Wagner., "The vapor-Liquid-Solid Mechanism of Crystal Growth and Its Application to Silicon", *Applied Physics Letters*, Vol.4, No.5, pp89-90, 1964.

[16]. A. Surawijaya, I. Anshori, A. Rohiman, and I. Idris. "Gold Nanoparticles Assisted Silicon Nanowire Growth using Vapor Liquid Solid Method". *AIP Conf. Proc.* 1415, p. 36, 2011.

[17]. Huang, F. Kim, A. R. Tao, S. Connor and P. Yang, "Spontaneous Formation of Nanoparticle stripe patterns through dewetting", *Nature Materials* Vol. 4, 2005, pp. 896-900.

[18]. DR. Divan, MA, D. C. Mancini, D. T. Keane, "Controlled X-Ray Induced Gold Nanoparticles Deposition", *Romanian Journal of Information Science and Technology*, Vol.11, No. 1, 2008, pp. 71-84.