Toward CMOS Process-Compatible Gold Nanoparticles Deposition with Pattern for Electronics Application

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Abstract: Two approaches in nanoscale device fabrication are the top-down and bottom-up approach. The later method promises application in VLSI technology but a major challenge existed: integration for other devices as well as electrodes. Described in this paper, we have optimized preparation process for photoresist coating and photolithography. Patterned gold-nanoparticles has been successfully deposited on top of a silicon substrate using positive photoresist as a mask. SEM characterization confirmed the presence of nanoparticles with average diameter of 55 nm while as EDS spectrum confirms the presence of gold nanoparticles on the patterned Si substrate.

Keywords: Gold nanoparticles, CMOS-compatible, photoresist, patterned deposition.

1. Introduction

Electronics device miniaturization has brought many advances in devices performance, such as an increase in speed, packing density, lower power consumption as well as cheaper manufacturing cost [1, 2, 3]. Intel and ST Microelectronics has demonstrated MOSFET with 15 nm of gate length [4, 5]. However, further device scaling is facing its limits due to the fact that parasitic effect will become more dominant which leads to degradation in device performance [6, 7, 8].

Several studies have been conducted in the field of the nanomaterials-based device [9]. Cui et.all [10] has successfully made an attempt in fabricating Silicon Nanowire Field Effect Transistor (SiNW FET) with a bottom gate where they use a 5 nm silicon nanowire as a channel connecting source and drain. The nanowires were grown by nanocluster-assisted growth method, then deposited on top of oxide layer via ethanol suspension.

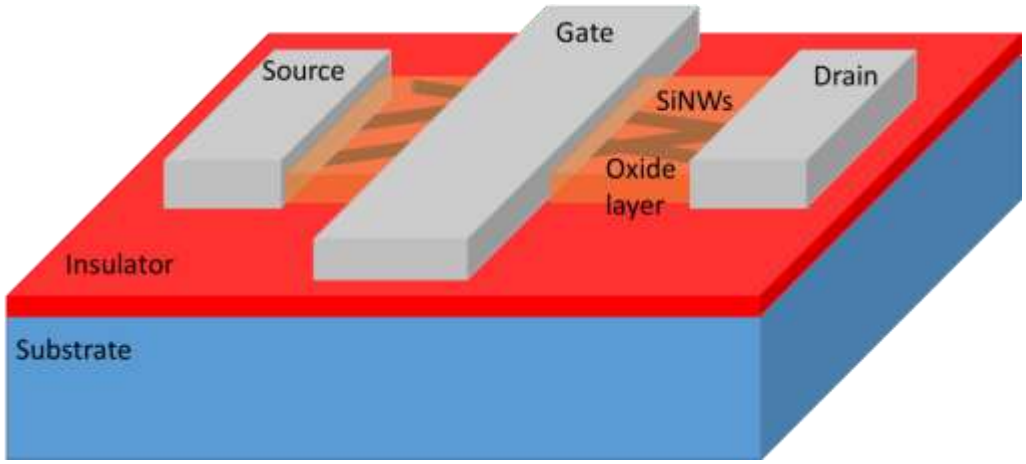

Figure 1. Schematic of a SiNW based FET

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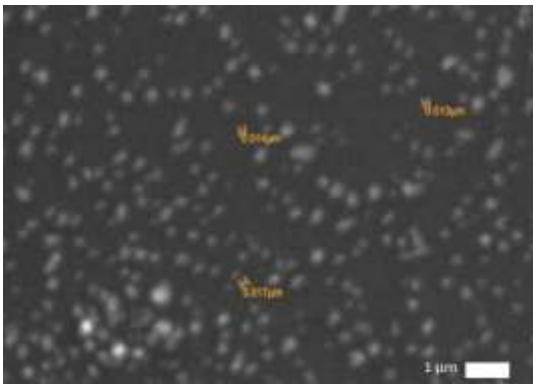
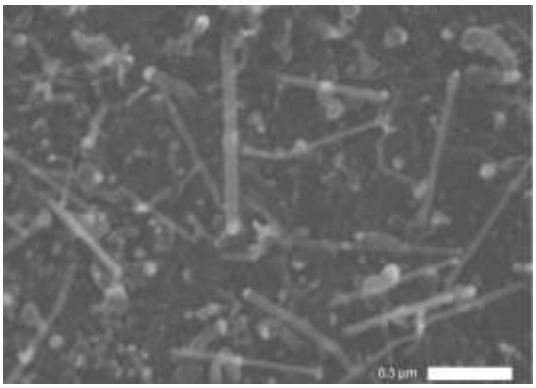
We plan to fabricate SiNW based FET using a top gate as shown schematically in Figure 1. We choose to use a top gate instead of a bottom gate to approach the conventional CMOS fabrication process. Also, using top gate will give a better performance like better subthreshold, higher transconductance and negligible hysteresis. Another advantage is that by using a top gate, SiNW surface will be covered by gate oxide preventing surface charge effect to influence the channel transconductance. As our first step in fabricating SiNW based CMOS, we begin by aligning SiNWs with metal contact by using patterned deposition of gold nanoparticles on top of the substrate. In this paper, we will discuss the patterned deposition of gold nanoparticles on top of a silicon substrate using conventional photolithography and dip coating method.

To extend the capability of device miniaturization, two common approaches are used, top-down and bottom-up approach. Top down approach is done by increasing the resolution of lithography in device fabrication. However, this approach will face constraints due to the limitations of lithography techniques which requires resolution to less than 5 nm, leads to very expensive cost [11]. To avoid the need for very high-resolution lithography in the fabrication of nano-sized structures, a technique to synthesize materials (nano-particle and nanowire) by so-called bottom-up approach is required.



(a)



(b)

Figure 2. SEM images of the previous result: (a) Gold nanoparticles deposited on a silicon substrate and (b) Silicon nanowires are grown using the gold nanoparticles as catalyst.

To synthesize nanoparticles, various techniques have been developed: mechanical approach (e.g. particle milling) or chemical approach (egg. Turkevich method and Plasma Enhanced Chemical-Vapor-Deposition). In Turkevich method which we used in this study, high purity

gold (99.99%) is dissolved in aqua regia to form a Chloroauric acid ($HAuCl_4$), which is then reduced with sodium citrate which results in gold nanoparticles (AuNP) [12, 13, 14].

In our previous study, we have successfully developed a method for preparing AuNPs using Turkevich method. The resulting gold nanoparticles have a diameter around 30 nm. By using dip coating method, we had successfully deposited AuNPs on a silicon substrate, and then use it as a metal catalyst to grow silicon nanowires using vapor liquid solid (VLS) method [15, 16]. The image of synthesized AuNPs and grown silicon nanowires is shown in figure 2. To be applied as functional electronic devices, integration with other devices to form an electronic circuit is necessary.

In this paper, we report a series of experiments to develop techniques to deposit AuNPs on a pattern on top of a silicon substrate. All experimental process is performed using standard CMOS process-compatible, with the goal that the developed technology can be easily integrated with existing standard CMOS process. Our research purpose is to establish a CMOS compatible process for SiNWs growth using patterned AuNP on a silicon surface to fabricate SiNWs based CMOS.

2. Methodology

In order to utilize silicon nanowires as functional electronics device, integration with electrodes and other VLSI device is required. There are two methods in nanowire integration. In batch methods, nanowires dispersed in an aqueous solution is deposited homogeneously on starting material. After the location is identified, the electrodes are fabricated on top of the nanowires location by using identification marker for alignment. The other method is based on the patterned growing of nanowire material, where nanowires can be grown on desired locations.

In order to deposit AuNPs on specific and predefined location, we use conventional photolithography to define patterns for the AuNPs location. Silicon substrate is coated with photoresist before AuNP deposition. This coating procedure is optimized so that the photoresist-mask will endure the deposition processes, such as dip-coating in AuNPs solution for more than 12 hours and dipping the sample in boiling water for the cleaning process. The photoresist on areas where AuNPs is designed to reside is then removed by means of a photolithography process.

3. Experimental, results, and discussion

To deposit AuNPs on samples, we used dip coating method which requires a sample to be dipped in an aqueous-based AuNP solution. Samples were coated with positive photoresist and then baked at 120^{o}C with different baking times. They were then dipped in colloidal nanoparticle solution for 6 hours. We found that only sample with less than 4 minutes baking time have its photoresist layer peeled off during the immersion.

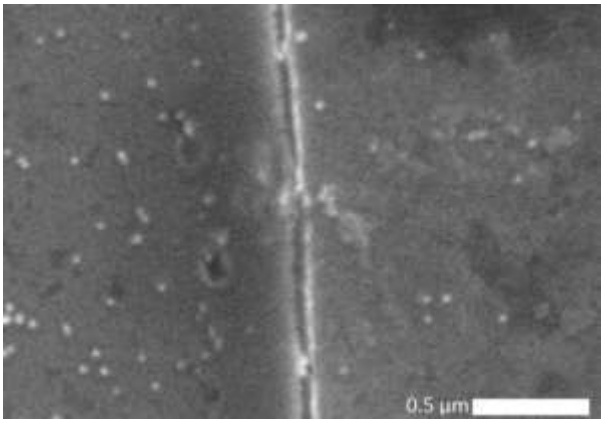
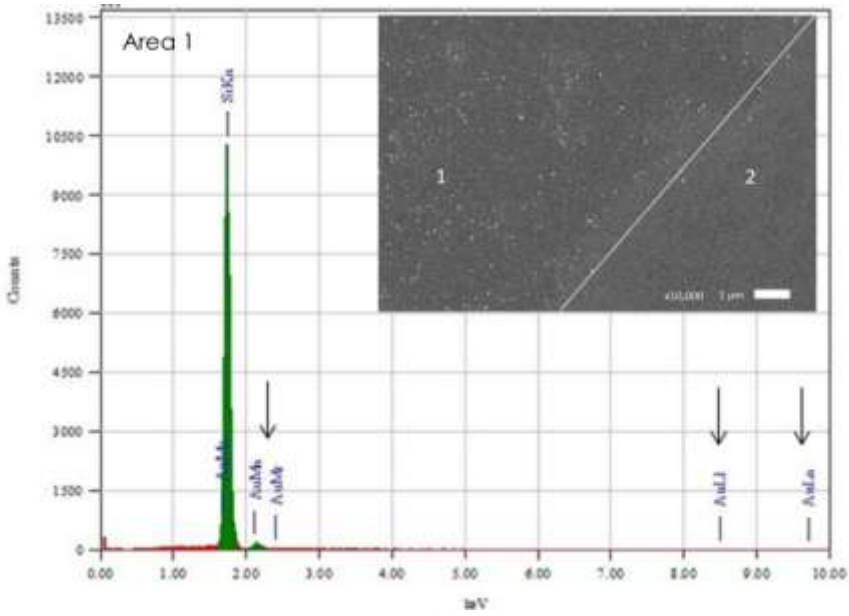
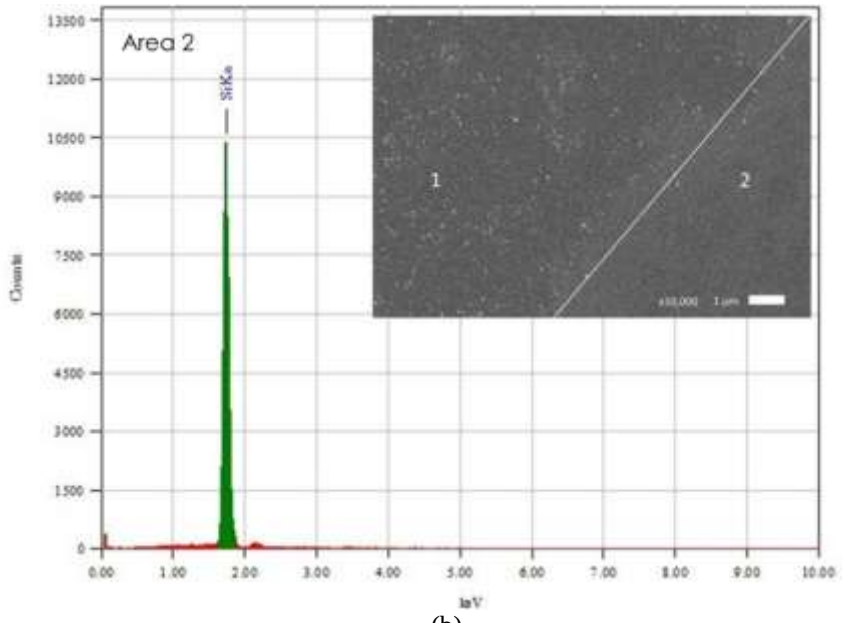


Figure 3. AuNPs successfully deposited on uncoated (left) and resist-coated (right) area.

Figure 3 shows the AuNPs deposited on the sample both on the area covered with photoresist and exposed area.



(a)



(b)

Figure 4. (a) EDS spectrum of area with AuNPs (b) EDS spectrum of area without AuNP.

Next experimental step is pattern development, which involves standard lithography process, from resist coating, pattern transfer via exposure and development. Silicon wafer is cleaned using standard RCA process and then coated with photoresist by spin-coating, and then baked at 80^{o}C for 3 minutes. Subsequently, the sample is baked at 120^{o}C for 8 minutes. We then proceed with dip coating process by immersing the sample in aqueous AuNPs solution for

6 hours, and finally rinsed in boiled water for approximately 5 seconds to remove NaCl remnants.

It turns out that the photoresist layer of a sample was peeled off while being rinsed in boiled water. It implies that strengthening the bonds between the photoresist layer and the silicon substrate is required so the photoresist layer could withstand the dip-coating and rinsing process. We then modify the fabrication steps by adding baking process before and after photoresist coating process, both of them done at 120^{o}C for 5 minutes. In addition, we also increase the post-bake time from 8 to 12 minutes, also at 120^{o}C. The sample fabricated using modified steps were proven to have photoresist layer with stronger bonding strength, even in boiled water.

As seen in figure 3, there is a clear difference in AuNps density on that two regions. We get AuNps density value of 19.2×10^{8} cm^{-2} on the uncoated area and 7.77×10^{8} cm^{-2} on the coated counterpart. Meanwhile, two other samples (a fully coated and fully uncoated one) show a much greater difference in density value, density calculation after lift-off process giving a result for the fully coated and fully uncoated of 0 cm^{-2} (no AuNps found) and 44.7×10^{8} cm^{-2} respectively. We expecting AuNps density counted to be 0 cm^{-2} instead of 7.77×10^{8} cm^{-2} on the coated area. This may occur as a result of rinsing processes following the dip coating stage. The acetone rinse (lift-off process) and boiled water bath are likely causing some AuNps to move from the uncoated to the coated area.

To increase the density of AuNPs deposited on the silicon substrate, we increase dip coating time to 12 hours. Using this recipe we then successfully deposited AuNPs on top of silicon substrate, both in area covered by photoresist and in area that was not. After resist stripping using acetone and DI water rinsing, the samples is then characterized using scanning electron microscope (SEM) and Energy Dispersive X-ray Spectroscopy (EDS). The result is shown in figure 4.

SEM observation confirmed the presence of AuNPs with an average diameter of 55 nm while as EDS spectrum shows the only Au (deposited material) and Si (substrate) were on the surface. The AuNPs density in area 1 is $2.1\text{x}10^{8}$ cm^{-2} while as in area 2 is counted only $0.4\text{x}10^{8}$ cm^{-2}. This value account to 1:5 density ratio. It is quite surprising since we expect that AuNps density will be proportional to dip coating time. Meanwhile, EDS result does give a distinct difference in Au mass percentage counted, in our previous sample (6 hours dip coat time) Au mass only account for 0.33% of total mass while the latter one reveal a 6.63% of Au mass. There are two possible reasons for this decrement in AuNps density. The first is the colloidal AuNps itself, we use the same colloidal AuNps in a different time where the second experiment was conducted 3 weeks after the first. Those time gap may give result in AuNps agglomeration inside the colloidal. Another possibility is distribution issue, as seen both in figure 3 and 4, AuNps are not uniformly distributed, it may give a chance to us to pick an SEM image in the low-density area.

Taking a density average from all of the samples above, we get AuNps density of 16.97×10^{8} cm^{-2} in the uncoated area as well as 2.1×10^{8} cm^{-2} in coated area. In other words, a ratio of 1:9 has been achieved. This quantitative result shows that patterned AuNps deposition has been successfully carried out.

Compared with other group activities such as Huang and Divan [17, 18], our process methodology is much simpler, hence we do not require complex tool such as Langmuir-Blodgett for the dip coating process. In contrast with other group material selection such as organic and polymer solvent (Toluene), we applied simpler process without any solvent to achieve acceptable AuNP deposition in patterned area.

4. Conclusion

In this paper, we have reported our experimental study in depositing AuNPs with a pattern on a silicon substrate using standard photolithography process. Optimization on resist preparation has been performed, and the result shows that AuNPs was successfully deposited on selected region of the wafer by dip coating method. An average density calculation reveals a

distinctive between AuNp density in the coated and uncoated area. The difference is in a ratio of 1:9. Our simpler methods and promising results have paved away for our next goal which is to synthesize SiNWs using deposited AuNPs as catalyst to fabricate self-aligned SiNWs for SiNW based FET.

5. Acknowledgement

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