A Switching Strategy of CHB Inverter for PV System Under Nonuniform Illuminating Conditions

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Abstract: This paper proposes a switching strategy for Cascaded H-bridge (CHB) multilevel inverter for photo voltaic (PV) power generation systems under nonuniform illuminating conditions. In order to minimize the switching frequency, selective harmonic elimination (SHE) technique is used to determine the inverter switching pattern. As the DC voltages are unbalanced and vary from time to time, the switching pattern has to change dynamically. How to implement the dynamic switching pattern by using a field programmable gate array (FPGA) is described in this paper. Several simulated and experimental results are included in this paper to show the effectiveness of the proposed method.

Keywords: dynamic switching; FPGA; SHE technique; unequal DC sources.

1. Introduction

Inverter is a key component in a photovoltaic (PV) power generation system. A brief description of inverter classification is shown in Figure1 [1],[2]. According to the dc source, an inverter can be classified into voltage-source inverter (VSI), and current-source inverter (CSI) [3],[4]. At present, VSI type is the preferred one compared to CSI [4],[5]. According to the output voltage level number, a VSI can be classified into 2-level voltage-source inverter and multilevel inverter (MLI). Moreover, the well-established topologies of wide variety of MLI are neutral point clamp (NPC), flying capacitor (FC), and CHB inverter [1],[6]. Among MLI topologies, the CHB has been accepted to be the most suitable candidate for the next generation PV system inverters [6]-[9]. The advantage of CHB inverters include modularity, fault tolerance, possibly use with unequal DC sources, and lower voltage stress of switch [1],[9]. A CHB inverter is composed by several H-bridge converters in cascade connection. The cascade topology allows the use of DC sources with equal (symmetric) as well as unequal (asymmetric) voltage values. To maximize energy capturing, some researchers propose PV system that uses multiple maximum power pont tracking (MPPT) [10],[11].

A CHB inverter is said to be symmetric if all DC sources have equal magnitude, otherwise the CHB inverter is asymmetric [2],[12]. Many pulse width modulation (PWM) techniques for CHB inverters were proposed in the literatures. Many PWM techniques eliminate some or all redundant states to increase the number of unique voltage levels which can be generated by the inverter [6],[13]. These PWM techniques were designed to work under predetermined unequal dc voltage sources. In PV power generation systems, the voltage level of each PV module is changing from time to time and cannot be predetermined. Thus, the existing PWM techniques may not work properly under these conditions.

This paper proposes a dynamic switching strategy for asymmetric CHB inverters. An FPGA is used to implement the proposed PWM technique. The proposed PWM techniques is based on SHE strategy. Simulated and experimental results show that the proposed PWM technique is effectively producing an output voltage with minimum harmonics.

This paper is organized as follows. Section 2 presents literatures review. Section 3 presents general description of the proposed method that includes principle of minimum staircase-sinewave gap area and algorithm of switching angles determination. Section 4 presents dynamic Switching of CHB inverter and the related switching strategy. Section 5 describes designing

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function blocks and optimizing the FPGA. In Section 6, simulation (MATLAB) and laboratory experimental results are presented. Besides, method validation is also discussed in this section by comparing those simulation and experimental results. Finally, Section 7 presents the summary and conclusion.

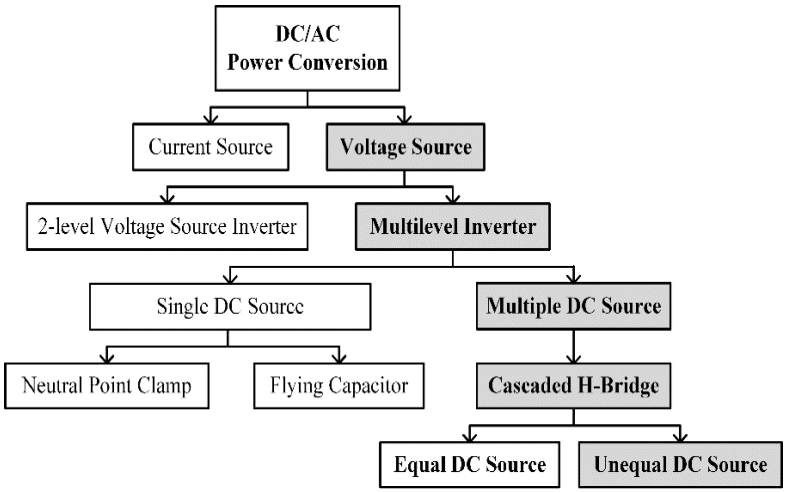


Figure 1. MLI classification [1].

2. Literatures Review

A comprehensive review of MLI topologies concerning well-established and emerging topologies as well as their modulation and control techniques are presented by [2]. This includes diode-clamped inverter, capacitor-clamped inverter, cascaded multicell inverter, generalized inverter, mixed-level hybrid multilevel cells, asymmetric hybrid multilevel cells, and soft-switched multilevel inverters. Moreover, this literature discribes systematically the related aspects such as evolution of MLI technologies, fundamental principles of various MLIs, and how MLIs have influenced commercial products, research and development.

Further developments, numerous variations and even combinations of those topologies have been presented to satisfy application requirements or to improve operation performances [1]. Recent topologies presented such as multiwinding transformer with single battery [7] in which stepped-waveforms resulted by H-bridge-multiwindings transformer are cascaded by output stages such that very high level staircase is produced; cascaded inverter fed by unequal DC sources topology [1] to which combination of turned-ON switches results high level output voltage waveform; cascaded MLI with variable and auxiliary DC source and floating capacitor (FC)(s) and high frequency link (HFL) to which composing a variable voltage and HFL voltages produces high level output voltage waveform [12]. Nevertheless, according to the authors in [13], MLI topologies with reduced power switch count have some compromises to pay such as increased voltage rating of semiconductor switches, requirement of bidirectional switches, loss of modularity, reduced number of redundant states, complex modulation schemes, etc. In this paper, only a taditional MLI that will be discussed, i.e. CHB topology. This topology is depicted in Figure 2.

Figure 2 shows general structure of CHB topology. Traditionally, CHB inverter is fed by equal DC voltage sources, but, in recent developments it have been modified by introducing unequal DC voltage source that so called asymmetry. A CHB inverter is an MLI formed by the series connection of two or more single-phase H-bridge inverters. In general terms, the CHB inverter output voltage is formed by those H-bridges, such that its total inverter output voltage as well as rated power are increased. Since CHB consists of m H-bridges, 2m+1 different voltage levels are obtained [1]-[3].

If proper modulation is applied in MLI, corresponding THD will compete with or better than PWM inverters [14]. A typical method using harmonic elimination principle is proposed by [15]. The principle adopted is more variable more harmonic order can be eliminated. For this purpose, it extends the possible variable of MLI. Number of such possible variable refers to setting of harmonic orders that will be eliminated. For which, unequal DC voltages are applied and added as additional variable. Then, to calculate such switching angles and unequal DC voltages, the corresponding nonlinear equations are solved offline.

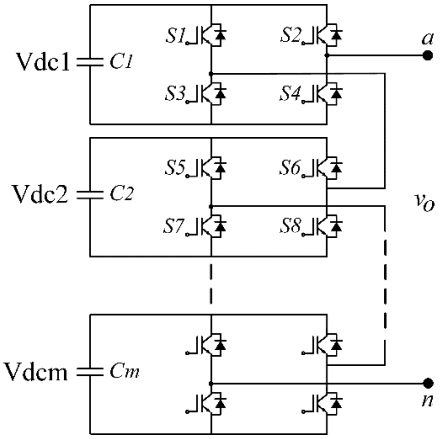


Figure 2. A traditional MLI topology [1]-[3].

Literature [16] proposes genetic algorithm (GA) technique to eliminate specified harmonic orders of MLI output voltage. The aim is to determine optimum switching angles that meets requirement of fundamental component and THD. The authors in [16] derive THD formula and specify objective function that includes required fundamental component and THD. In which, GA is performed to minimize objective function. Moreover, the obtained solution will result optimum switching angles.

The authors in [14] propose analytical procedure for SHE in five-level inverter operating at fundamental frequency. Their proposed method calculates all possible switching angles eliminating a specified odd harmonic from the output voltage. Such a method solves the SHE system equations, i.e. first and second equation which corresponds to switching angles function and modulation index, respectively. In this case, computations are performed by conventional microprocessors and DSPs together with a closed loop controller.

A good method of decoupling AC against DC component from SHE system equations have been proposed by [17]. Furtermore, this literature presents comprehensively decomposing such system into its components, i.e. steady state switching angles, switching angle perturbations, steady state amplitude fundamental harmonics, and amplitude perturbations of harmonic orders that will be eliminated. Through those derivations, then, the corresponding nonlinear equations are converted into a specific control system in which difficulties of solving high order nonlinear transcendental equations in SHE technique to be overcome.

Literature [18] describes a unified approach extending modulation indices ranges particularly the lower range in which switching angles exist. Such a method transforms SHE system equations that chracterizes nonlinear transcendental into a single set of symmetric polynomial. The complete set of solutions to this polynomial equations are found using resultant theory. Based on a typical THD formula, the smallest THD obtained are plotted with a wider range of modulation indices. This procedure results sets of switching angles as a function of modulation index stored in a lookup table.

To meet grid codes under unequal voltage due to SHE not performing optimally when DC link imbalance, [19] proposes selective harmonic mitigation pulsewidth modulation (SHM-PWM) that capable of preprogramming the harmonic profile of the output waveform over a range

of modulation indices. Based on the different sets of angles stored in lookup tables (LUTs), the proposed method performs interpolation such LUTs to find switching angles for specific situations, in this case, DC link imbalance. Such interpolation principle refers to intercell imbalance sharing of DC link. In this method, the corresponding equations can be solved offline and the solution computed by a DSP on demand.

To enable control of both reactive power and voltage of individual capacitors in a cascaded H-bridge based static VAR vompensator (CHB-STATCOM), [20] introduces SHE technique with asymmetry topology. The reactive power and capacitor voltage are controlled by utilizing decoupled current control and unequal DC-link voltages with SHE, respectively. In this case, unequal DC-link voltage will increase voltage level, and in turn, improve the quality of output waveform. Firstly, [20] transforming voltage equations of CHB-based STATCOM from the *abc* stationary frame into the *d-q* synchronous frame to obtain voltage and current components in *dq* frame. Then, asuming *d*-axis of the *d-q* reference frame is aligned to *a*-axis of *abc* frame, active and reactive power reference can be determined for controlling independently. A supplementary control system is required for desired voltage (or unequal values) of individual DC-links. Whereas, by utilizing asymmetric DC voltages with SHE, inverter output THD is improved.
Comprehensively, facing unequal DC voltages problem, such abovementioned SHE techniques utilize switching angles stored in LUT(s) instead of performing real time computation. For instance, the method in [18] uses a set of selected switching angles stored in LUT. These selected switching angles are correlated to the lowest THDs due to nonsingle SHE solution. It should be noted that THD is computed using typical THD formula derived by [18]. Whereas, a method in [19] calculates switching angles through interpolating LUTs containing switching angle values to obtain the closest switching angles.

Because DC voltages vary randomly, utilizing LUT(s), whether direcly or not, may result unacceptable solutions. This paper proposes preconditioned SHE technique that includes preconditioning SHE system equation based on principle of minimum staircase-sinewave gap area; and performing real time switching angles computations. The aim of these techniques are to achieve THD requirement, to accommodate real time situations, and also to accomplish success commutations. To actualize these aims, dynamic switching is performed. Then, solving such system equation, generating switching signals, as well as controlling switches are carried out by an FPGA. The more detailed description of both staircase-sinewave gap area and dynamic switching are presented in Section 3 and 4.

3. General Description

The main idea of this paper is maximizing captured energy of PV system facing DC voltage variations, wether its magnitudes are uniform or not, by controlling CHB inverter switching angles. Because PV modules operate at their maximum power points (MPPs), generated DC voltages may be unequal due to nonuniform conditions. Accordingly, a strategy proposed is exploiting those unequal DC voltages such that resulting better output waveform, i.e. near sinewave. Furthermore, it is assumed that the corresponding PV modules operate at their MPPs and will not discussed. Figure 3 shows schematic diagram of 9-level CHB inverter utilized in this study. In addition, each cell of the CHB inverter is fed by an isolated DC source to avoid short circuit [9],[19]. Whereas DC sources are generated by PV system. Hereafter, PV system is represented by DC sources. Consequently, intercell power imbalance may occur due to nonuniform condition to which have been given the attention of many studies. To analyze this impact, unlike most studies, this paper intends for unequal DC voltage rather than unequal phase current approach [21]. This impact includes DC voltages equalization, symmetric or asymmetric topology option, as well as modulation technique which this paper focuses on.

The MLI reproduces sinewave through staircase composed by DC voltages. Based on Fourier series expansion, SHE technique generates system equations with eliminated certain harmonics. If iteration is used to solve such equations, the problem usually faced is determining initial guess [14],[18],[19]. This study proposes precondition step to avoid difficulty of determining initial

guess as well as shorten the iteration cycles. This step based on principle of staircase-sinewave gap area which is discussed in the following subsection.

Several modulation techniques can be used to control a CHB inverter [1]-[3],[6]-[9],[12]-[21] but, as aforementioned, the SHE technique is applied in this paper. In this case, SHE technique eliminates 5th, 7th, and 11th harmonic order from the corresponding equations of stepped-waveform recomposed by staircase-sinewave gap area principle. Such equations are dealing with staircases synthesized by sequenced DC voltage magnitudes. Consequently, dynamic switching algorithm should be performed to implement the proposed method.

A. Staircase-sinewave Gap Area

To conceive the idea of the proposed method, considering Figure 4 which illustrates staircases composed by typical unequal DC voltages, Vdc_is, and its switching angle θ_i ($i=1,2,3,4$), respectively, where $Vdc_1 > Vdc_3 > Vdc_2 > Vdc_4$. Figure 4(a) shows a resulted staircase without arranged switching angles, ($\theta_1 < \theta_2 < \theta_3 < \theta_4$), whereas Figure 4(b) shows a resulted staircase with arranged switching angles, ($\theta_1 < \theta_3 < \theta_2 < \theta_4$). These mean gap areas formed by staircase and sinewave can be changed through controlling conducting angles. The staircase at which minimum gap area achieved is the closest stepped-waveform to the sinewave. If staircase-sinewave gap area $\approx$ ½ x $\sum_{i=1}^{i=n} \Delta A_i$, the smallest gap area can be found by comparing $\sum_{i=1}^{i=n} \Delta A_i$ each other. Each gap area formed is a function of switching angles, i.e. $\Delta A_i = Vdc_i$ x ($\theta_{i+1} - \theta_i$). According to Figure 4, the corresponding gap area without and with arranged switching angles are ΔA_i ($i=1,2,3,4,5$) and $\Delta A_i'$ ($i=1,2,3,4,5$), respectively. Because the curve of $v_{PQ}(\omega t)$ between $0-\pi/2$ and $\pi/2-\pi$ is symmetry, taking $0-\pi/2$ period, comparison of $\sum_{i=1}^{i=5} \Delta A_i$ and $\sum_{i=1}^{i=5} \Delta A_i'$ can be described as follows.

$$\sum_{i=1}^{i=5} \Delta A_i = \Delta A_1 + \Delta A_2 + \Delta A_3 + \Delta A_4 + \Delta A_5$$

$$\sum_{i=1}^{i=5} \Delta A_i = \theta_1 Vdc1 + (\theta_2 - \theta_1)Vdc2 + (\theta_3 - \theta_2)Vdc3 + (\theta_4 - \theta_3)Vdc4 + (\pi/2 - \theta_4)(Vm - \sum_{1}^{4} Vdci) \quad (1)$$

$$\sum_{i=1}^{i=5} \Delta A_i' = \Delta A_1 + \Delta A_2' + \Delta A_3' + \Delta A_4 + \Delta A_5'$$

$$\sum_{i=1}^{i=5} \Delta A_i' = \theta_1 Vdc1 + (\theta_2' - \theta_1)Vdc2 + (\theta_3' - \theta_2)Vdc3 + (\theta_4 - \theta_3')Vdc4 + (\pi/2 - \theta_4')(Vm - \sum_{1}^{4} Vdci) \quad (2)$$

$$\theta_2 = \sin^{-1}\left(\frac{Vdc1 + Vdc2}{Vm}\right) \quad (3)$$

$$\theta_3 = \sin^{-1}\left(\frac{Vdc1 + Vdc2 + Vdc3}{Vm}\right) \quad (4)$$

$$\theta_4 = \sin^{-1}\left(\frac{Vdc1 + Vdc2 + Vdc3 + + Vdc4}{Vm}\right) \quad (5)$$

$$\theta_2' = \sin^{-1}\left(\frac{Vdc1 + Vdc3}{Vm}\right) \quad (6)$$

$$\theta_3' = \sin^{-1}\left(\frac{Vdc1 + Vdc3 + Vdc2}{Vm}\right) \quad (7)$$

$$\theta_4' = \sin^{-1}\left(\frac{Vdc1 + Vdc3 + Vdc2 + Vdc4}{Vm}\right) \quad (8)$$

$$\sum_{i=1}^{i=5} \Delta A_i - \sum_{i=1}^{i=5} \Delta A_i' > 0$$

$$\sum_{i=1}^{i=5}\Delta A_i^{'} < \sum_{i=1}^{i=5}\Delta A_i \tag{9}$$

From (9), it can be seen that the smaller staircase-sinewave gap area is obtained when synthesized waveform is composed by sequenced voltage magnitudes, i.e. $\theta_1^{'} < \theta_2^{'} < \theta_3^{'} < \theta_4^{'}$. In this case , $\theta_1^{'}$, $\theta_2^{'}$, $\theta_3^{'}$ and $\theta_4^{'}$ are switching angles of Vdc_1, Vdc_3, Vdc_2, and Vdc_4, respectively.

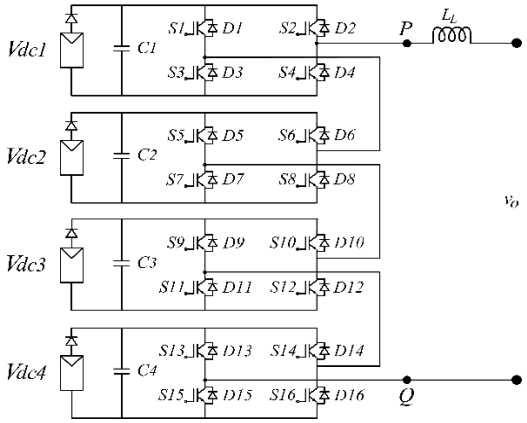


Figure 3. Schematic diagram of 9-level CHB inverter with unequal dc sources (V_i s).

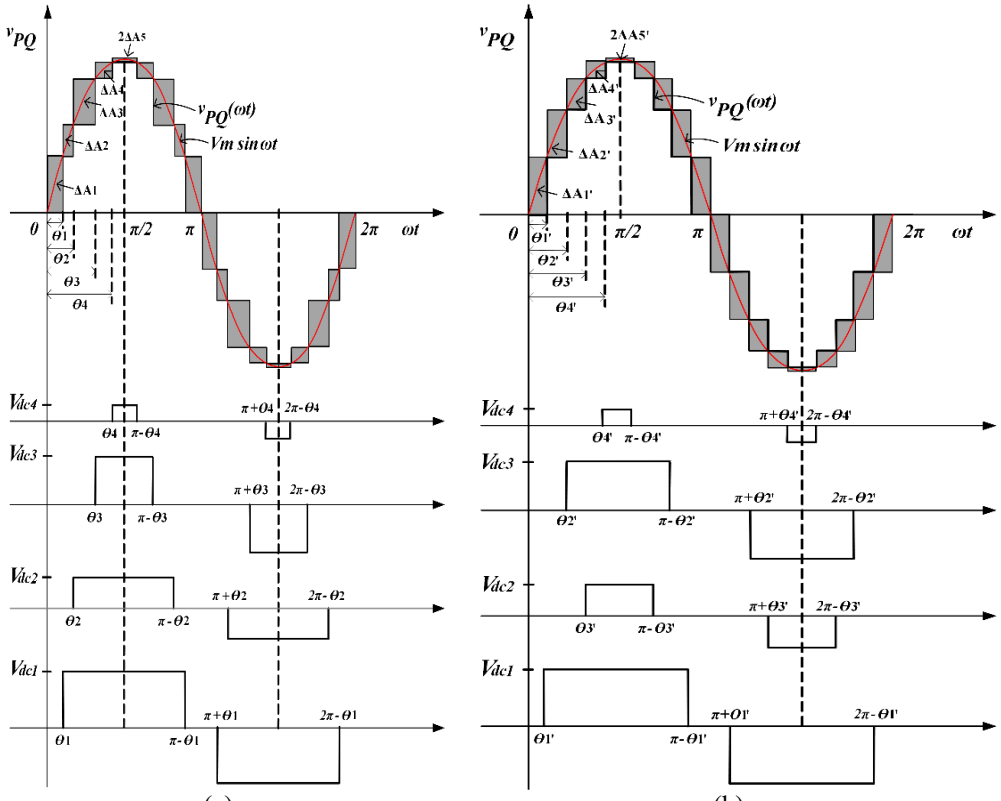


Figure 4. Typical CHB inverter output voltage generated by unequal dc voltages. (a) A waveform that corresponds to physical topology switching, and (b) a waveform that corresponds to logical topology switching.

B. Dynamic Switching Algorithm

Figure 4 demonstrates output voltage waveform of a CHB inverter composed by unequal DC voltages. Comparing Figs. 4(a) and (b), it can be seen that different switching angles show different waveshapes. Figs. 4(a) and (b) are correlated to the physical topology (the switching based on switches lay-out scenario) and the logical topology (the switching based on sequent DC cell-magnitudes scenario), respectively.

The SHE technique decomposes a result staircase into its square waveform components and analyses it using Fourier series to find switching angles [1],[2],[7]-[9], [12]-[21]. As can be seen in the graphs, turn-ON and turn-OFF of each switch is once in a cycle, in other words, the active power switch is commutated one time within a cycle, therefore, such a modulation is classified into low switching technique.

Dynamic switching algorithm sorts those unequal DC voltages, composes staircase, analyses corresponding stepped-waveform, generates SHE system equations and, finally, finds switching angles. Such sorting DC voltages includes recomposing $v_j(t) = Vdc_j$ with θ_j for $j \in \{1,2,..m\}$ into $v_i(t) = Vdc_i$ with θ_i and $Vdc_i > Vdc_{i+1}$ for $i \in \{1,2,..m\}$. Where $v_j(t)$, $v_i(t)$, θ_j, and θ_i are unarranged DC source, arranged DC source, switching angle of unarranged DC source, and switching angle of arranged DC source, respectively.

Considering stepped-waveform Figure 4(b), instead of Figure 4(a) which each square waveform component can be represented by (10). Recomposing unarranged $v_j(t) = Vdc_j$ results $v_i(t) = Vdc_i$, i.e. Vdc_1, Vdc_2^{new}, Vdc_3^{new}, Vdc_4. To find each unknown switching angle, θ_i, this entire stepped-waveform can be written into (11) and further development will result (12). In these equations, fundamental harmonic, V_1, is maintained and the significant harmonics, i.e. 5th, 7th, and 11th, are eliminated. Furthermore the system (12) should be developed, whose characteristics are nonlinear trancendental, by applying steps (12)-(14). In this case, J is Jacobian. Solving such equations, Newton-Raphson iteration is applied to find those switching angles, θ_i s.

$$f(x) = a_0 + \sum_{n=1}^{\infty}(a_n \cos nx + b_n \sin nx) \tag{10}$$

$$v_{V_{dc1}}(\omega t) + v_{V_{dc2}^{new}}(\omega t) + v_{V_{dc3}^{new}}(\omega t) + v_{V_{dc4}}(\omega t)$$

$$= \sum \frac{4}{n\pi}\left(V_{dc1}\cos n\theta_1 + V_{dc2}^{new}\cos n\theta_2 + V_{dc3}^{new}\cos n\theta_{dc3} + V_{dc4}\cos n\theta_4\right)\sin n\omega t \tag{11}$$

$$f(\theta) = \begin{bmatrix} \frac{4}{\pi}(V_{dc1}\cos\theta_1 + V_{dc2}^{new}\cos\theta_2 + V_{dc3}^{new}\cos\theta_3 + V_{dc4}\cos\theta_4) - V_1 \\ \frac{4}{5\pi}(V_{dc1}\cos 5\theta_1 + V_{dc2}^{new}\cos 5\theta_2 + V_{dc3}^{new}\cos 5\theta_3 + V_{dc4}\cos 5\theta_4) \\ \frac{4}{7\pi}(V_{dc1}\cos 7\theta_1 + V_{dc2}^{new}\cos 7\theta_2 + V_{dc3}^{new}\cos 7\theta_3 + V_{dc4}\cos 7\theta_4) \\ \frac{4}{11\pi}(V_{dc1}\cos 11\theta_1 + V_{dc2}^{new}\cos 11\theta_2 + V_{dc3}^{new}\cos 11\theta_3 + V_{dc4}\cos 11\theta_4) \end{bmatrix} \tag{12}$$

$$\theta_{q+1} = \theta_q - J^{-1}f(\theta_q) = \theta_q - \Delta\theta_q \tag{13}$$

$$J=\begin{bmatrix} -\frac{4}{\pi}V_{dc1}\sin\theta_1 & -\frac{4}{\pi}V_{dc2}^{new}\sin\theta_2 & -\frac{4}{\pi}V_{dc3}^{new}\sin\theta_3 & -\frac{4}{\pi}V_{dc4}\sin\theta_4 \\ -\frac{4}{\pi}V_{dc1}\sin 5\theta_1 & -\frac{4}{\pi}V_{dc2}^{new}\sin 5\theta_2 & -\frac{4}{\pi}V_{dc3}^{new}\sin 5\theta_3 & -\frac{4}{\pi}V_{dc4}\sin 5\theta_4 \\ -\frac{4}{\pi}V_{dc1}\sin 7\theta_1 & -\frac{4}{\pi}V_{dc2}^{new}\sin 7\theta_2 & -\frac{4}{\pi}V_{dc3}^{new}\sin 7\theta_3 & -\frac{4}{\pi}V_{dc4}\sin 7\theta_4 \\ -\frac{4}{\pi}V_{dc1}\sin 11\theta_1 & -\frac{4}{\pi}V_{dc2}^{new}\sin 11\theta_2 & -\frac{4}{\pi}V_{dc3}^{new}\sin 11\theta_3 & -\frac{4}{\pi}V_{dc4}\sin 11\theta_4 \end{bmatrix} \quad (14)$$

Algorithm of switching angles determination is outlined briefly in Figure 5. For which, every cell voltage, $v(t) = \left[Vdc_1^{new}, Vdc_2^{new}, Vdc_3^{new}, ..., Vdc_m^{new}\right]$, should be measured in the real-time. These cell voltages are then rearanged and composed for further analysing. Such rearranged cell voltages are $Vdc_1^{new}, Vdc_2^{new}, Vdc_3^{new}, ..., Vdc_m^{new}$, where $Vdc_1^{new} > Vdc_2^{new} > Vdc_3^{new} > ... > Vdc_m^{new}$.

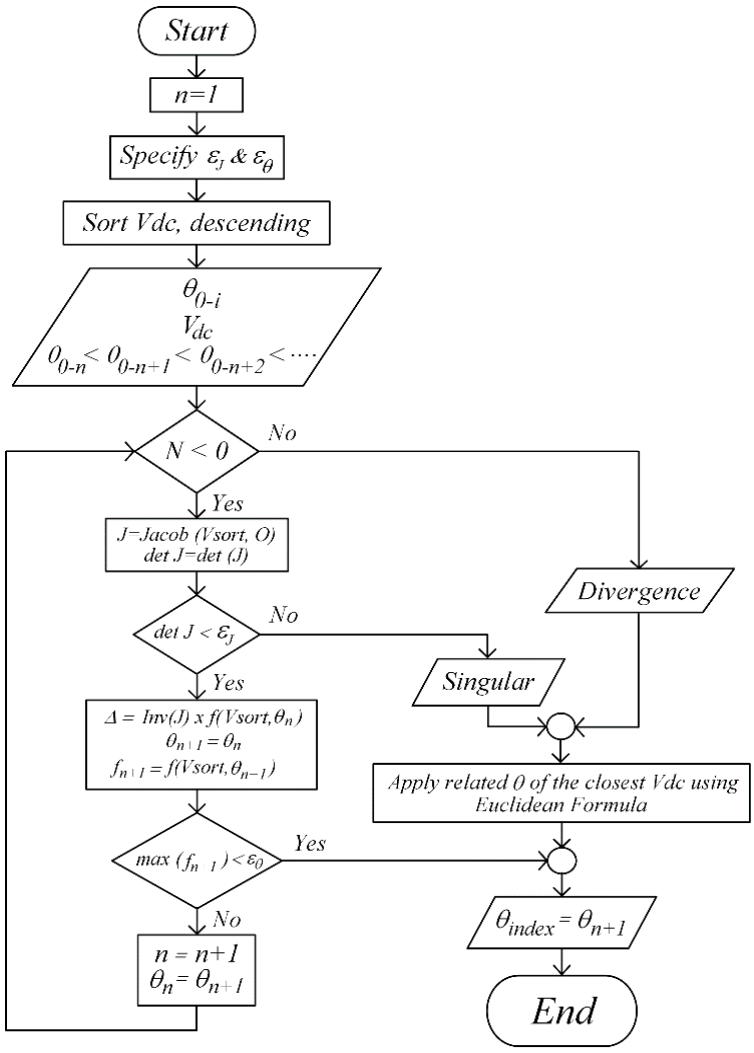


Figure 5. Switching angles computation.

There are two indicators should be quantified in this iteration i.e. ε_J and ε_θ that corresponds to Jacobian determinance, *det J*, and switching angle function, $f(Vdc_i, \theta_i)$, respectively.

$$0 \le \left|\det J\right| < \varepsilon_J \tag{15}$$

$$0 \le \left|f(Vdc_i, \theta_i)\right| < \varepsilon_\theta \tag{16}$$

Since (15) is satisfied, then the iteration is continued due to nonsingular matrix. Whereas, since (16) is satisfied, the values of switching angles are obtained so that iteration cycles can be ended. However, if (15) is not satisfied and the iteration cycles are more than predetermined limit, these indicating that the matrix is singular and the iteration process is divergence. For these cases, the switching angle uses the closest cell voltages' switching angle computed by Euclidean inner product in *m*-space, R^m, formula [22] as written by (17).

$$d(\mathrm{u,v}) = \|\mathrm{u\text{-}v}\| = \sqrt{\langle \mathbf{u}-\mathbf{v}, \mathbf{u}-\mathbf{v} \rangle} \tag{17}$$

$$\mathrm{u} = (u_1, u_2, u_3, \ldots u_m) \tag{18}$$

$$\mathrm{v} = (v_1, v_2, v_3, \ldots v_m) \tag{19}$$

In the above equations, d(u,v), u, v, u_i (i=1,2,3…m), and v_i (i=1,2,3…m), are distance between vector u and vector v, vector u, vector v , ordinate of u, and ordinate of v in Euclidean *m*-space, respectively. Hence, the proposed method overcomes the problem of both singular matrix and divergent iteration.

4. Dynamic Switching and Commutation

To implement switching scenario of rearranged DC voltage magnitudes as aforementioned, CHB inverter should be able to perform dynamic switching whose switching patterns based on logical topology instead of physical topology. Figure 6 shows typical dynamic switching to generate a stepped-waveform shown in Figure 4(b) that involves transferring current of switches. Considering Figures. 6(b) and (g), to generate $V_{PQ} = Vdc_1 + Vdc_3$ and $V_{PQ} = -Vdc_1 - Vdc_3$, respectively, switches connected to positive and negative voltage of DC sources #1 and #3 are turned-ON, whereas the other switches are turned-OFF. Such switching patterns or current paths of a sinewave shown in Figure 4(b) are depicted by Figs. 6(a)-(i).

To obtain voltage level $V_{PQ} = V_{dc1}$ as shown in Figure 6(a), S2, S3, S7, S8, S11, S12, S15, and S16 are turned-ON whereas the others are turned-OFF. Correspondingly, at the beginning, the turning-ON switches are S3, S4, S7, S8, S11, S12, S15, and S16. Figs. 7(a) and (b) show the ON-state switches and its simplified equivalent circuit, respectively. Since a filter (L_L) is applied at the output of inverter, transferring the load current from one switch to another will not take place instantly. Regarding to Figure 7, a process of transferring load current from S4 to S2 is shown by Figure 8(a). Assuming at t = 0^-, the load current is I_L, S2 is OFF, and S4 is ON. As the S2 to be switched ON, i_{S2} does not instantly equal I_L because of L_L. Consequently, S4 must remain ON while the current in S2 increases to that of the load. The interval when both S2 and S4 are ON is called the commutation angle or commutation time [23].

Assume $v_o = V_m \sin \omega t$, when both S2 and S4 are ON, the voltage across L_L is

$$v_{L_L} = V_m \sin \omega t \tag{20}$$

and the current in L_L is $i_L = \dfrac{1}{L_L} \int_0^{\omega t} V_m \sin \omega t d\omega t$

$$i_L = \frac{V_m}{\omega L_L}(1 - \cos \omega t) + i_L(0) \tag{21}$$

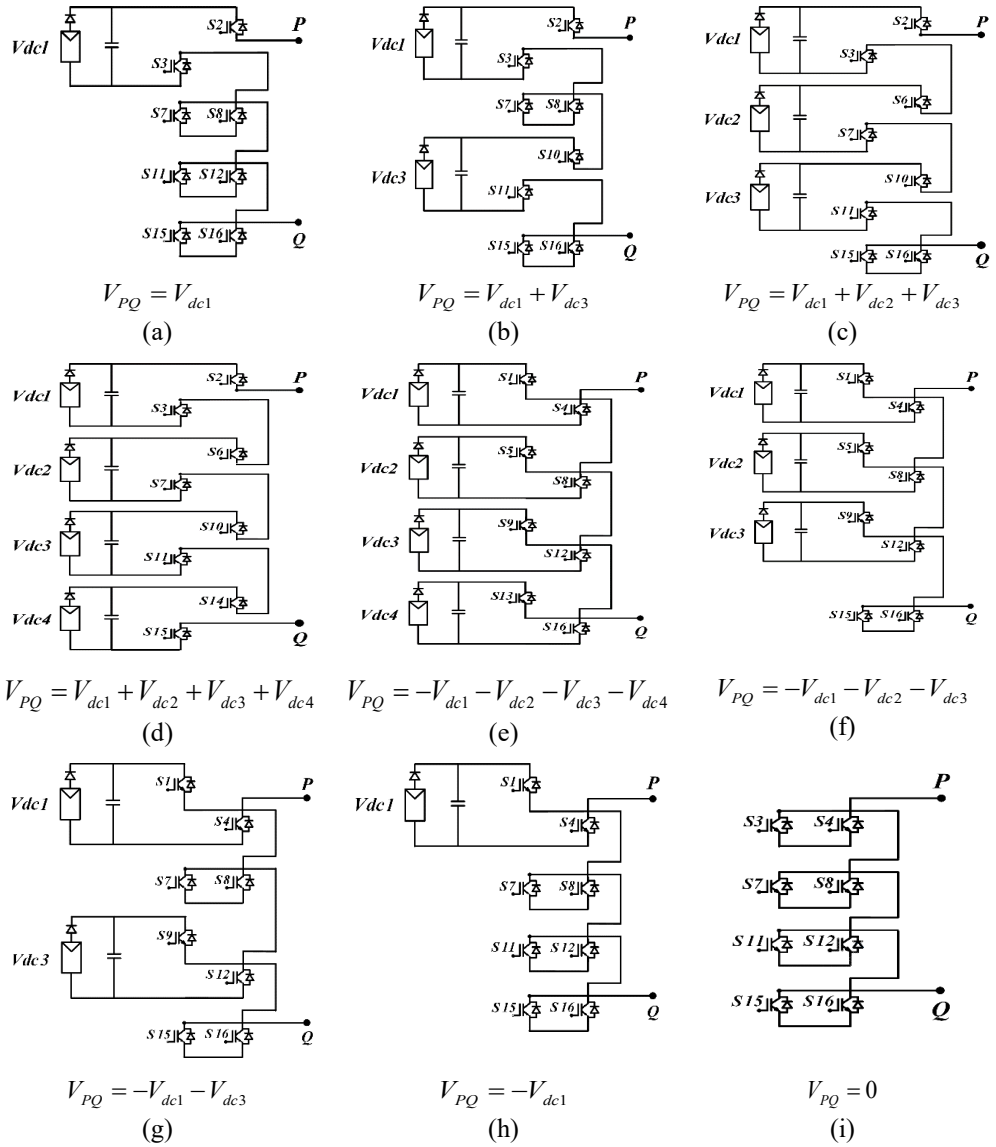


Figure 6. Typical patterns of dynamic switching.

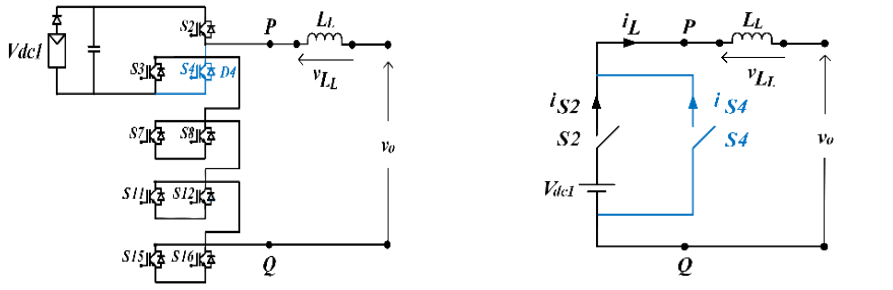


Figure 7. Current path during commutation process of Figure 6(a). (a) A circuit corresponding DC source connected and switches turned-ON, and (b) the simplified equivalent circuit of Figure 7(a) expressing current path.

$$i_L = i_{S2} + i_{S4} \tag{22}$$

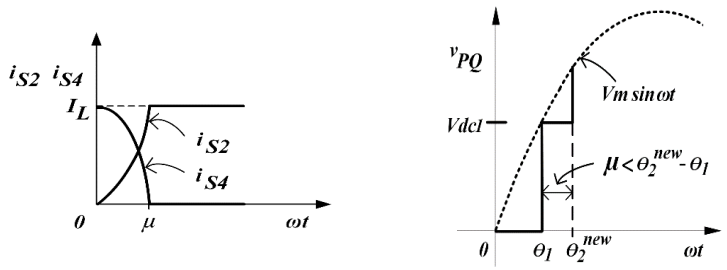
$$i_{S4} = i_L - \frac{V_m}{\omega L_L}(1-\cos\omega t) + i_L(0) \tag{23}$$

Letting the angle at which i_{S4} reaches zero be $\omega t = \mu$. Solving for μ,

$$\mu = \cos^{-1}\left(1 - \frac{\boldsymbol{i_L \omega L_L}}{\boldsymbol{V_m}}\right) \tag{24}$$

Equation (24) shows that commutation angle, μ, can be calculated according to the load and or filter reactance, L_L, amplitude of sinewave, V_m, and load current, i_L and has nothing to do with the firing angle of other switches.

Hence to ensure commutation successfully, inductance L_L and amplitude V_m of expected output sinewave should be taken into account. In addition, commutation is successful if the commutation taking place between switch S2 firing angle, θ_1, and the next switch firing angle, θ_2^{new}.



(a) (b)

Figure 8. The process of commutation. (a) Transfering load current from S4 to S2, and (b) synthesizing load voltage.

Applying this method, the iteration process will be simpler and also the problem of guessing initial values can be avoided. However, these may effect the switches commutation. An FPGA is applied to realize on both implementing dynamic switching and avoiding commutation failure.

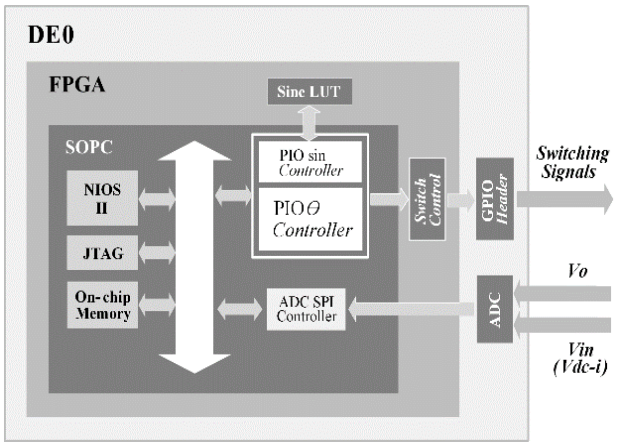
5. FPGA Implementation

As abovementioned, there are three scenarios of switching angles computation considered, i.e. convergent iteration, divergent iteration, and singular matrix. In case of convergent iteration, it refers to (13), whereas beyond this, either divergent iteration or singular matrices it refers to (17). To limit consuming time which affects the inverter response time, maximum of each iteration is limited to be 200 cycles. Whereas, the iteration cycle is satisfied when a switching angle deviation, max f_{n+1}, is less than predetermined error, $\mathcal{E}_j$. In this study either $\mathcal{E}_j$ or $\mathcal{E}_\Theta$ is specified to be 10^{-6}. On the contrary, if iteration has reached 200 cycles but max f_{n+1} is still higher than $\mathcal{E}_j$ the iteration process is stopped then Θ_n (s) uses the closest voltage calculated by the Euclidean formula.

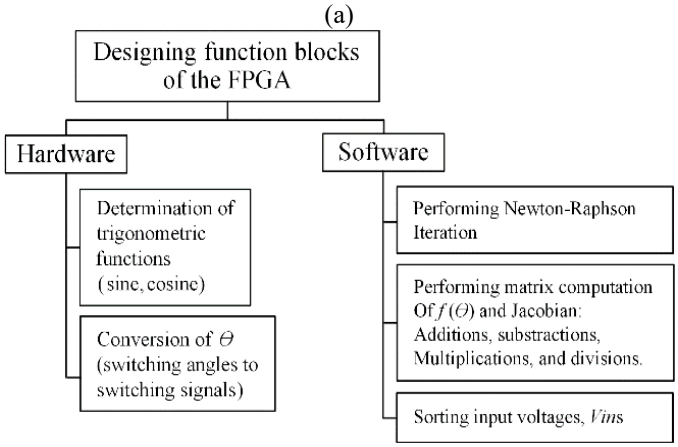
An FPGA performs those iterations to find switching angles, θ_i s, and controlling switches. To which, the resulting switching angles are translated into switching signals to turn-ON/OFF 9-level CHB inverter switches. Due to limited capacity of both logic cell and memory, the FPGA should be configured to maximize its functionality. Dealing with FPGA burden, the principles taken into account are the more resouces needed the more complicated if such functions are fully performed by hardware, contrariwise the more consuming time needed if those are fully performed by software. Hence, its optimized configurations are as follows:

- Iteration functions covering great many inversion, multiplications and division operations are carried out by software.
- Calculations of main trigonometric function such as sine Θ and switching angles to switching signals conversion are carried out by hardware.

Hence, accommodating these trade offs, further optimizations include both configuration and architecture of the FPGA can be summarized in Figure 9. Figure 9(a) illustrates work flow of signal processing where an SOPC block is generated, a lookup table (sine LUT) and a switch control are created and located outside the SOPC block. Furthermore, NIOS II, JTAG, on chip memory, ADC SPI, and PIO controller are generated in the SOPC block. The FPGA proccesses voltages delivered by PV modules to generate switching signals that be used to turn-ON/OFF switches. To obtain these switching signals, both switching angles computations and switching angles conversions should be accomplished. Those switching angles computations are performed by the NIOS II whereas sin Θ values are provided by sine LUT. Figure 9(b) shows detailed function block comprising hardware and software. Table 1 shows switching states of CHB inverter whose states can be translated into switching signals.



(a)



(b)

Figure 9. FPGA implementation. (a) Architecture of the FPGA, and (b) Hardware and software configuration.

A. Hardware

There are 2 parts of hardware designed in the FPGA, i.e. sine LUT and switch control as described by Figure 9(a). There are 1024 addresses (=2^{10}) allocated for 0- $\pi/2$ range to sine LUT, and for accomodating 0.0015 radian of Θ incremental whereas beyond this range and other

trigonometric functions are performed by software using the appropriate values. Once resulting θ_i s, i.e. $\theta_1 - \theta_4$, are obtained, the respective switching signals can be generated.

B. Software

The main substructure functions of the proposed software design comprise read ADC, Newton-Raphson iteration, and write θ. Whose computations such as $f(\theta)$, Jacobian, inversion, sin θ (beyond the provided sine LUT), and cos θ, are performed in the Newton-Raphson substructure as described by (12)-(14).

The clock signal of the FPGA and the desired inverter output voltage are 50 MHz and 50 Hz, respectively. These mean transformation ratio of the FPGA to power grid is 1,000,000 (=50 MHz/50 Hz). So that, it takes 1.000.000 clocks to achieve a cycle of sine waveform, in other word 2π of voltage waveform in a grid equals 1,000,000 clocks in the FPGA. Therefore, such a switching angle, $0 \le \theta < \pi/2$, in 50 Hz equals $0 \le \theta < 250.000$ clocks in 50 Mhz domain.

6. Simulation and Experimental Results

Simulation under MATLAB software and laboratory experiments are carried out to examine the proposed method. In this case, the unequal DC sources include *m* ratio from 0.75 to 1.00, where $m = V_m / \sum V_{dci}$, V_m and $\sum V_{dci}$ are amplitude of expected sinewave and summation of DC source magnitudes, respectively. The MATLAB simulation performs iterations to find the switching angles, generate stepped-waveforms, and calculate the THD%. Once switching angles are obtained, gating switches can be modelled. Table 1 and Figure 10 show the model of these gating signals to turn-ON/OFF switches to synthesize a stepped-waveform.

Well-defined objectives of inverter design involve such as minimizing size, minimizing losses, or a combination of them [24],[25], but this paper focuses more on THD% rather than these objectives. The THD% is related to power quality issues as part of interconnection standard. Because the inverter is connected to the grid, it must meet utility company standards, besides International standard such as IEEE 519-2014, IEC61727, etc. which should be considered [6]. Equation (25) shows the THD% formula used in this study.

$$THD = \frac{\sqrt{\sum_{n=5,7,11,\ldots}^{49} V_n^2}}{V_1} x100 \qquad (25)$$

In above equation, V_1, V_n, and n are root mean square (RMS) of fundamental frequency voltage, RMS of *n* order harmonic voltage, and order harmonic, respectively.

A. Simulation Results

Figure 11 shows fast-Fourier-transform (FFT) spectrum of output voltage waveforms resulted by simulation in MATLAB. This graph clearly demonstrates the harmonic content of resulted waveform, i.e. 5th, 7th, 11th harmonic orders are eliminated, corresponding to the SHE technique, and also triplen and even harmonic are excluded, due to 3-phase application and quarter-wave symmetry, respectively. Figure 11(a) demonstrates harmonics content resulted by unequal DC sources for m = 1 whereas Figure 11(b) resulted by unequal DC sources for m = 0.75. In particular, such graphs reveal its significant harmonic distortions, i.e. 13th, 17th, 19th, 23th, 25th, 29th, 31th, 37th, 41th, 43th, 47th, and 49th order. It should be noticed that those profiles are simulated-characteristics where selected harmonics, i.e. 5th, 7th, 11th order, even, and triplen harmonics are excluded.

B. Experimental Results

Figure 12 shows hourly solar radiation obtained by direct measurement at ITB campus, Bandung (Indonesia) on January 1, 2017. It can be seen that solar irradiance changing from time

to time. In turn, this changed solar irradiance affects PV modules voltage. Moreover, this correlation is considered by both simulation and laboratory experimental.

It says that the THD was calculated for a 3-phase system. However, the experiment was performed with a 1-phase system. Figures 13(a) and (b) show the laboratory experimental configuration and a prototype of 9-level CHB inverter, respectively. In this experiment, Tektronix (TDS 2022B) osciloscope and Fluke (43B) power quality analyzer are used to record staircase waveform and to measure output voltage THD%, respectively.

Table 1. Typical switching states of 9-level CHB Inverter.

Voltage Magnitude	Switch ON (=1)/OFF (=0), (S#)																Switching angle
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	
0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	
Va	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0	Θa
Va+Vb	0	1	1	0	0	1	1	0	1	1	0	0	1	1	0	0	Θb
Va+Vb+Vc	0	1	1	0	0	1	1	0	0	1	1	0	1	1	0	0	Θc
Va+Vb+Vc+Vd	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	Θd
Va+Vb+Vc	0	1	1	0	0	1	1	0	0	1	1	0	1	1	0	0	Π-Θd
Va+Vb	0	1	1	0	0	1	1	0	1	1	0	0	1	1	0	0	Π-Θc
Va	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0	Π-Θb
0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	Π-Θa
-Va	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	Π+Θa
-Va-Vb	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1	Π+Θb
-Va-Vb-Vc	1	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1	Π+Θc
-Va-Vb-Vc-Vd	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	Π+Θd
-Va-Vb-Vc	1	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1	2Π-Θd
-Va-Vb	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1	2Π-Θc
-Va	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	2Π-Θb
0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	2Π-Θa

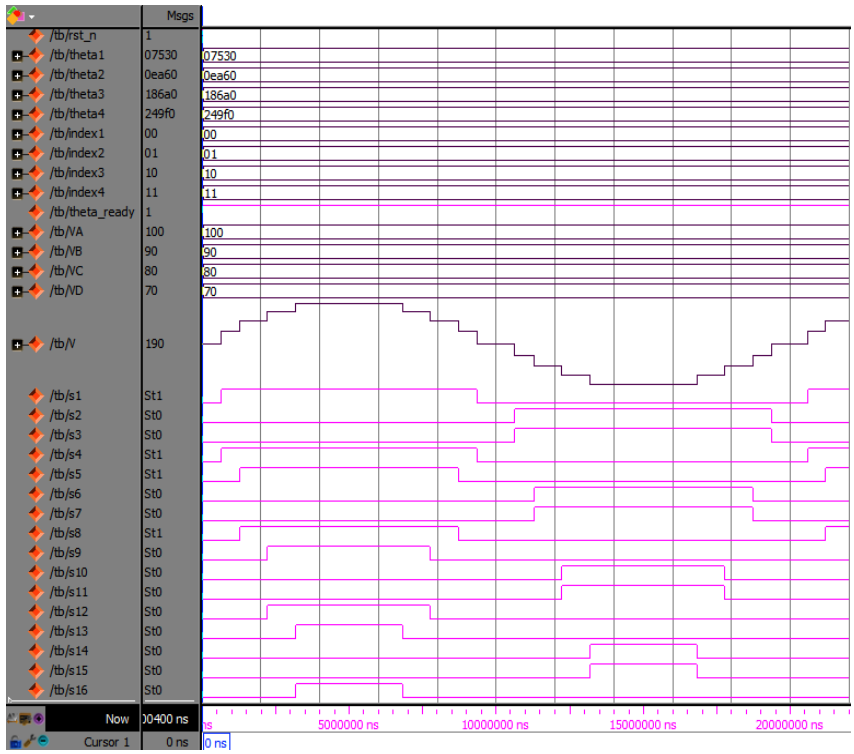


Figure 10. Switching signals model (S1 to S16) to compose stepped-waveform voltage of 9-level CHB inverter.

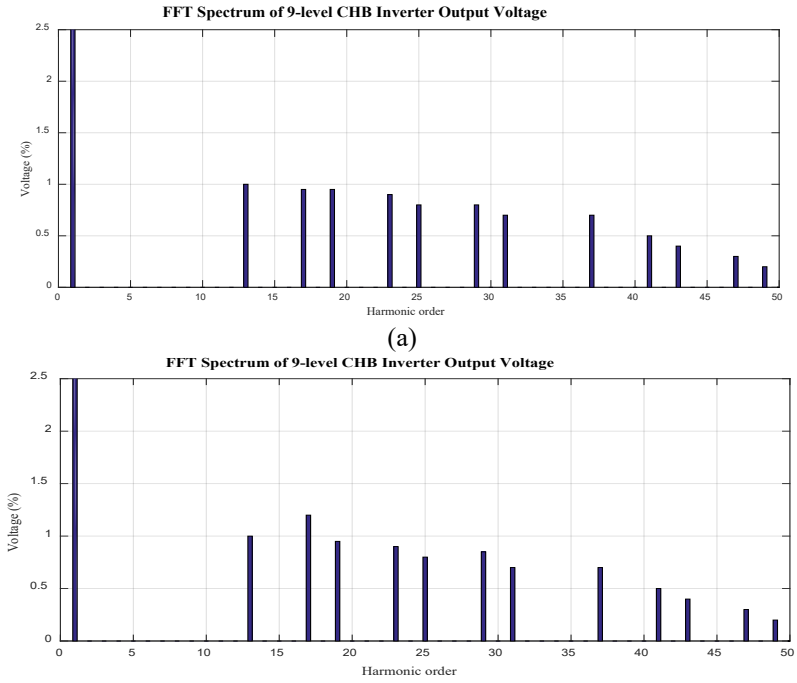
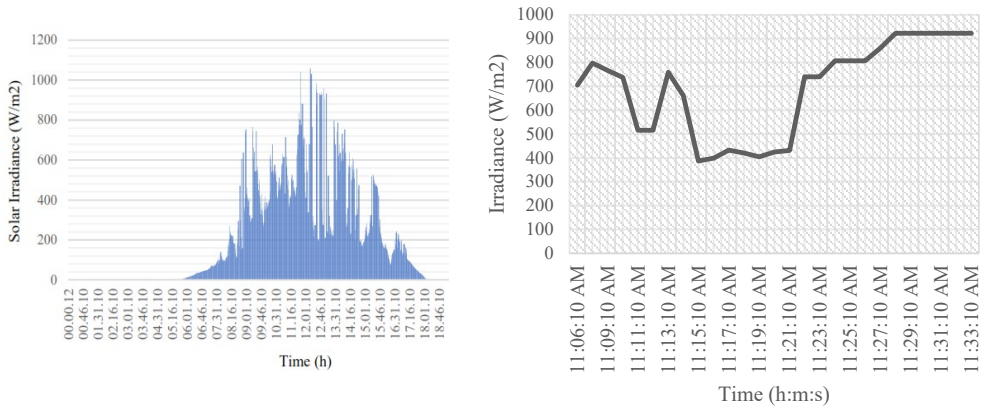


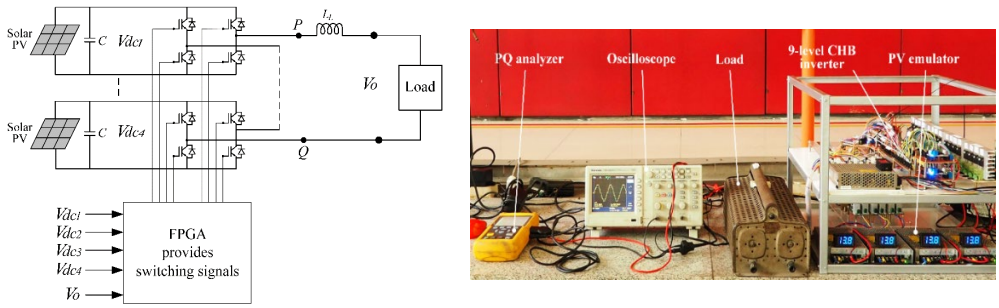
Figure 11. Output voltage FFT spectrums of 9-level CHB inverter based on simulation where 5th, 7th, 11th order eliminated and also triplen and even harmonics are excluded. (a) FFT spectrums related to CHB fed by unequal DC sources with m = 1, and (b) FFT spectrums related to CHB fed by unequal DC sources with m = 0.75.

Figures 14 (a)-(d) show the experiment results of CHB inverter fed by both equal and unequal DC sources with different m value, i.e. m = 0.96 and m = 0.80. For unequal DC sources and equal DC sources with m 0.96 were obtained by magnitudes composition (108V, 100V, 92V, 84V) and 96V(s), respectively. Similarly, for unequal DC sources and equal DC sources with m 0.80 were obtained by magnitude composition (88V, 82V, 78V, 72V) and 80 V(s), respectively. In this case, V_m was 400V.



(a) (b)

Figure 12. Typical hourly solar irradiance (W/m^2). (a) Solar irradiance measured on January 1, 2017 at ITB campus, Bandung, Indonesia, and (b) Zooming in Figure 10(a), between 11:06:10 and 11:33:10.



(a) (b)

Figure 13. The laboratory experimental test. (a) Schematic diagram, and (b) prototype of 9-level CHB inverter with the related experiment set.

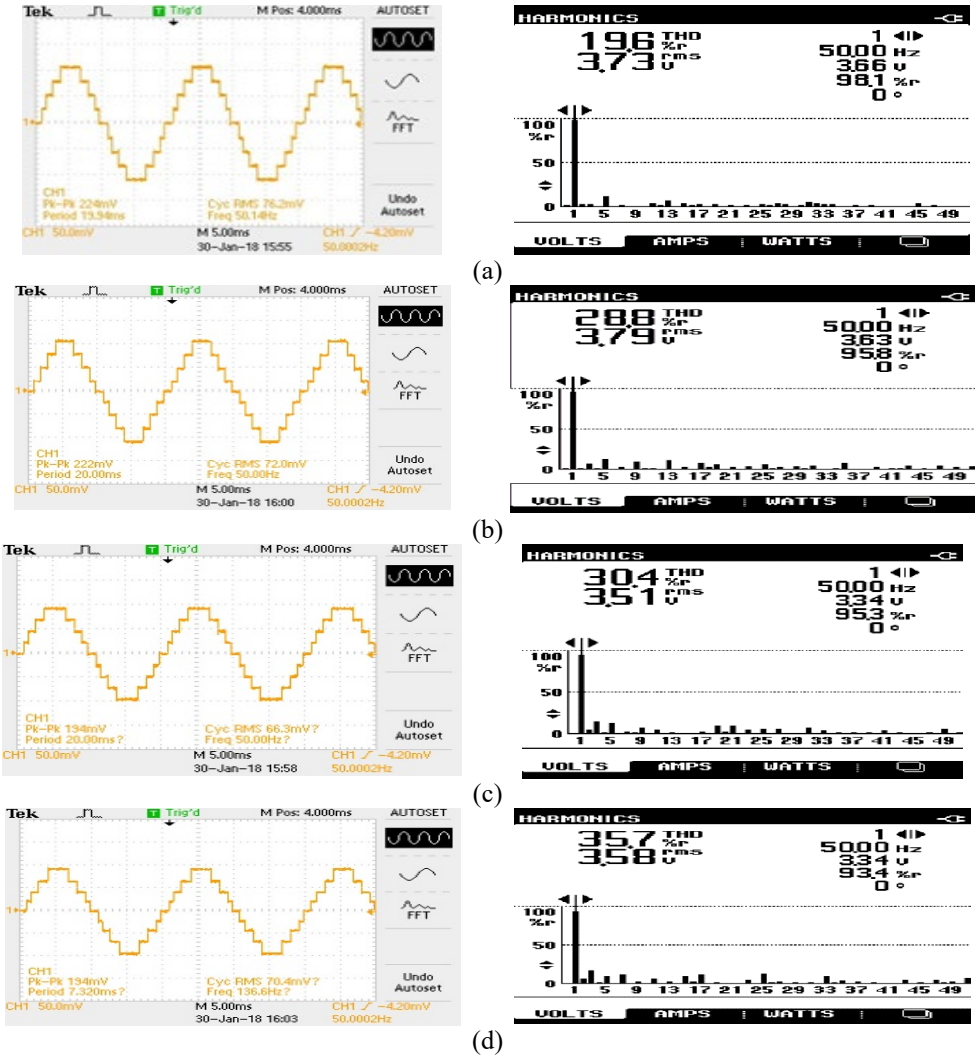


Figure 15. 9-level stepped-waveforms (Tektronik TDS 2022b) and THD%s (Fluke 43B) of CHB inverter output voltage resulted by the laboratory experimental test. (a) The output related to unequal DC voltages (108V, 100V, 92V, 84V), *m* 0.96; (b) the output related to equal DC voltages (96V), *m* 0.96; (c) the output related to unequal DC voltages (88V, 82V, 78V, 72V), *m* 0.80; and (d) the output related to equal DC voltages (80V), *m* 0.80.

From these graphs, it can be seen that the switch commutations are taking place successfully. Whereas, in general, THD%s measured show quite high which are confirmed by the corresponding recorded harmonic spectrums. It should be noted, these measured THD%s are including both even and triplen harmonics such that confirm those recording spectrums. Hence, these THD%s should be adjusted for consistency with their design as given by (25). Hereafter, adjusted THD%s are attributed as experiment THD%s. Such experiment THD%s correlating to Figs. 15(a)-(d) to be 5.78% 6.76%, 7.80%, and 7.95%, respectively. Then, the comprehensive THD%s based on experiment and simulation can be depicted by Fig. 15. Figure 15 shows those experimental results are confirmed by simulation results. From Figure 15 can also be seen that 92% of the THD%s according to both simulation and experiment meet the IEEE 519-2014 standard [26], [27], i.e. THD% ≤ 8%.

Finally, to evaluate the effectiveness of the FPGA design and utilization, in Table 2 is shown utilization summary dealing with. As can be seen, percentage of pin usage is 75% therefore the rest of the FPGA capacity can still be used to 3 phase application purpose for which needs additional 32 pins.

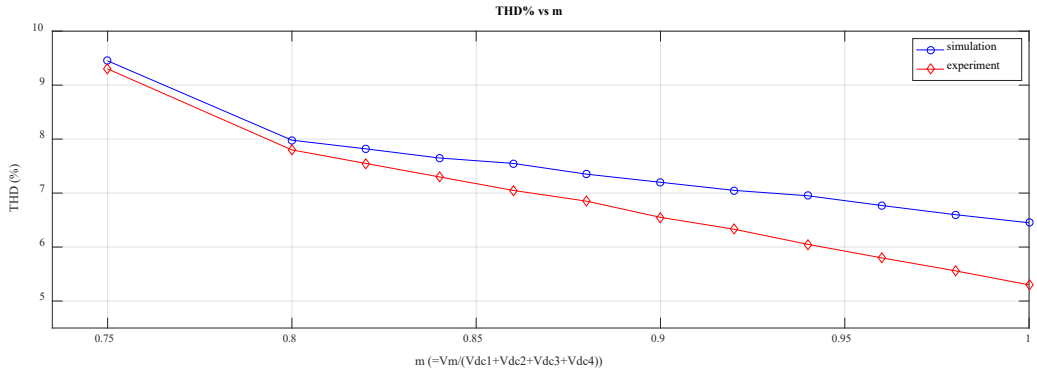


Figure 15. THD% comparison between simulation and laboratory experimental.

Table 2. The FPGA Utilization summary.

Resource	Available	Utilization	Utilization (%)
Logic elements	22.320	9.305	42
Pins	154	116	75
Memory bits	608.256	441.440	73
Embedded multiplier 9-bit elements	132	16	12

7. Conclusion

A switching strategy of CHB inverter fed by unequal DC voltage representing PV system under nonuniform illuminating condition is proposed. The use of an FPGA on performing iteration as well as controlling switches shows its capability on avoiding commutation problem and achieving expected output voltages, i.e. stepped-waveform approaching sinewave. Moreover, THD% of CHB inverter output voltage based on simulations and experiments show the most results meet IEEE 519-2014 standard, i.e. THD% ≤ 8%. In addition, utilizations of the FPGA to perform those algorithms have been discribed and show in such good percent capacities. In order to examine such reliabilitiy of the proposed method, further study proposed is implementing it in the real nonuniform illuminating conditions.

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