A Transformerless DSTATCOM Based on Cross-Switched Multilevel Inverter for Grid Voltage Regulation

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Abstract: In this paper, a transformerless distribution static synchronous compensator (DSTATCOM) based on the cross-switched (CS) multilevel inverter (CSMLI) is introduced. In comparison with the well-known cascaded h-bridge (CHB) topology, CS inverter produces higher number of voltage levels using fewer number of power components. Since CS inverter produces ac side voltage with high quality and has the ability to work at high voltage and power levels, the proposed CS-DSTATCOM is directly connected to the distribution grid without the need for a transformer. In the proposed CS-DSTATCOM, all the dc sources are replaced with dc capacitors. In this paper, an effective voltage balancing control scheme is proposed to keep the capacitors voltages balanced in the CS structure. The control scheme balances the capacitors voltages in two levels, i.e., inter-cell and within-cell level. On the other hand, the over-voltage and under-voltage phenomena are of the most common power quality (PQ) issues in distribution grids. The proposed DSTATCOM is able to cope with these issues by exchanging reactive power with the grid. Applying the CSMLI in the DSTATCOM structure as well as the capacitors voltage balancing methods are the main novelties of the paper. Also, the capacitors values are considered to be different (which is unavoidable in practice) while their voltages are balanced using the proposed voltage balancing methods. In this paper, a CS-DSTATCOM has been designed for 11 kV distribution grid and several simulation results are provided in the MATLAB/Simulink environment which validate the feasibility and performance of the proposed CS-DSTATCOM.

Keywords: static synchronous compensator (STATCOM), cross-switched multilevel inverter, voltage balancing scheme, transformerless converter.

1. Introduction

In weak distribution power networks where the series impedance of the system feeders is considerable, the voltage drop on the line impedance yields the voltage of the receiving end of the feeders to be out of the acceptable tolerance. As a popular solution, the distribution static compensator (DSTATCOM) is used to compensate reactive power and hence reduce voltage drop on the feeders [1]. For the DSTATCOM in distribution voltage levels (20kV, 11kV, 6.6kV, etc.), there are two commonly used options; the DSTACOM based on the conventional three-phase inverter with transformer and that based on the multilevel inverter without transformer. The transformer-less DSTATCOM is interested because of lower cost and size, and also high-quality ac side waveforms. However, multilevel structures with more power electronic components increase the control and modulation system complexity.

Application of the conventional multilevel inverters in the STATCOM or DSTATCOM has been widely studied in the literature [1-7]. In [2] analysis and implementation of a 6.6kV STATCOM based on the hybrid CHB inverter along with its capacitors voltage balancing has been presented. In [3], a modified selective harmonic elimination technique has been proposed for a CHB-STATCOM in which the switching angles are determined in such a way that the capacitors voltages are kept balanced. In [4], the operation of CHB-STATCOM under grid fault condition is investigated in which both positive and negative-sequence reactive currents are controlled during grid faults. Also, the operation of CHB-STATCOM under faulty condition in the power switches is studied in [5] where a fault tolerant approach is presented to

ensure the continuous operation of CHB-STATCOM after switch failures. In [6], a feedforward control has been presented for the delta-connected CHB-STATCOM where the zero sequence circulating current in the delta loop is used to provide cluster balancing. The application of the diode-clamped modular multilevel converter as the STATCOM is studied in [7]. In this study, employing a voltage clamping technique, the capacitors voltage balancing is achieved with fewer voltage sensors. In [8], a CHB-STATCOM is presented with a low dc side capacitance. In this paper, the theoretical calculation of the required capacitance is presented and it is indicated that the large voltage ripple on the dc voltages does not necessarily jeopardize the output current quality. The mitigation of high-order voltage and current harmonics is challenging because of the fact that a wide bang gap system is required. This is accomplished by a modular multilevel converter based STATCOM in [9]. A different voltage balancing approach for a CHB-STATCOM is presented in [10]. In this work, special attention has been paid to unbalanced grid voltage condition. A new control scheme is introduced to the limit the STATCOM peak current under unbalanced grid voltage. Analysis and control of the delta-connected CHB-STATCOM, applied for load imbalance and voltage flicker compensation is presented in [11]. The effect of switching harmonics on the instantaneous power sharing on the DC capacitors and hence their voltage balance in a CHB-STATCOM has been studied in [12]. Application of a current source modular multilevel converter as a DSTATCOM has been studied in [13]. The coupling effect of the individual voltage balance controller on the voltage and current controller of a CHB-STATCOM is studied in [14] in which a decoupled control system is presented to eliminate the coupling effects. In [15] the individual phase current control (to cope with the unbalanced grid condition) of a CHB-STATCOM is presented where the control is based on the optimal determination of the current components. The two conventional capacitors voltage balancing methods in a CHB-STATCOM (i.e. negative sequence current and zero-sequence voltage) are integrated in [16] by introducing a factor that is selected by the user. The zero-sequence voltage injection method for DC capacitors voltage balancing in a CHB-STATCOM under unbalanced grid condition has been studied in [17]. A passivity-based nonlinear current controller is applied on the CHB based transformerless STATCOM in [18]. The controller also considers the voltage balancing of the capacitors. In [19], the state feedback control strategy considering the capacitors voltage balancing has been presented for the CHB-STATCOM. The DC capacitors voltage balancing of a diode-clamped inverter based STATCOM using the multilevel space-vector pulse-width modulation (SVPWM) has been presented in [20]. On the other hand, several multilevel inverter structures have been introduced in the literature which use reduced power electronic switches at the expense of losing modularity [21, 22]. Cross-switched (CS) multilevel inverter presented in [20, 21] is an innovative topology in which a compromise between the number of switching devices and the modularity is made.

Due to its advantages, a CS based DSTATCOM is presented in this paper, and its design and voltage balancing scheme is investigated. The CS inverter has not been used in the STATCOM or DSTATCOM application and hence its capacitor voltage balancing issue has not been investigated before. It is worth noting that several dc voltage sources have been used in the structure of the CS multilevel inverter; however, in this paper, they are replaced by the capacitors. A hierarchical voltage balancing scheme is proposed to control dc side voltages in two control levels, i.e., inter-cell and within-cell levels. The rest of this paper is organized as follows. In section 2, the circuit configuration of the proposed CS-DSTATCOM is presented and its output voltage synthesis is discussed in section 3. The control system of the DSTATCOM is presented in section 4 followed by the dc voltages balancing scheme presented in section 5. The design procedure of the 11kV DSTATCOM based on the CS multilevel inverter is given in section 6. The simulation verification of the proposed CS-DSTATCOM and the proposed dc capacitors voltage balancing method is presented in section 7.

2. Circuit Configuration of The CS-DSTATCOM

The distribution static compensator is a power-electronic converter-based device used to regulate the grid voltage and control reactive power of the grid. In fact, the proposed DSTATCOM is a CS multilevel inverter connected to a grid in parallel at the point of common coupling (PCC). The CS inverter uses fewer number of power components for a certain number of output voltage levels compared to conventional inverters. The CS inverter produce output voltage with high quality and low harmonic contents. Due to its modularity, CS inverter can operate at high voltage and power levels [23].
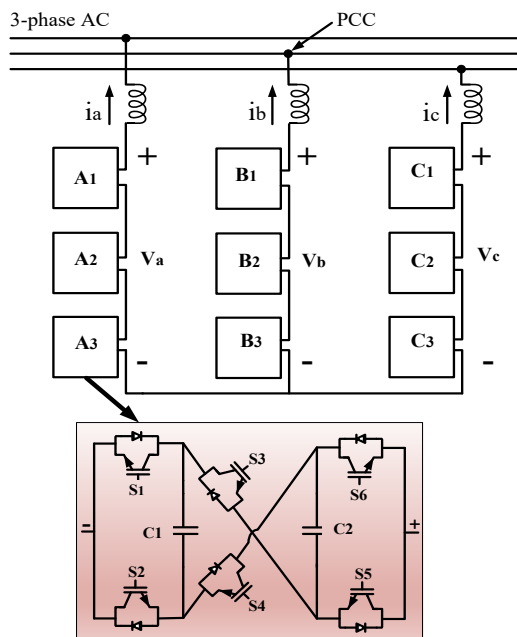

Figure 1. Circuit configuration of the three-phase 11kV DSTATCOM based on cross-switched multilevel converter.

Figure 1 shows the circuit configuration of a DSTATCOM based on a 13-level CS inverter that is connected to a three-phase distribution grid at the PCC. This converter consists of three clusters with star configuration and each of the clusters consists of three series-connected basic units. Since the structure of the CS multilevel inverter is modular, each basic unit can be installed as a separate module in clusters. As shown in Figure 1, a basic unit includes a CS 5-level inverter which consists of 2 capacitors and 6 power electronic switches. The proposed CS-DSTATCOM is designed for a 11kV system, however, it can also be applied for 20kV distribution systems by increasing the number of basic units in a cluster in a way that the 17-level or 21-level inverter can be used for 20kV system. In the CS-DSTATCOM circuit configuration, each cluster acts as a single-phase converter and three clusters together form a three-phase converter.

3. Output Voltage Synthesis

The output voltage of each phase in the CS-DSTATCOM is generated by the voltage sum of the series basic units. Each basic unit produces a 5-level voltage and each cluster produces a 13-level voltage. The CS output voltage has a low harmonic content, so there is no need to install a passive shunt filter at the ac side. The CS switching algorithm is based on phase shift pulse width modulation (PS-PWM) technique [24]. In this technique, six triangular carrier signals (between zero and one) are used for each cluster, and the carrier signals are selected so that they have a phase difference of 60 degrees. These carriers are compared to the

corresponding reference waveform in order to generate the switching signals of the outer switches (e.g. S1, S2, S5 and S6 in Figure 1). In fact, these switches operate at high frequency (equal to the carrier frequency) and their blocking voltage is the same as the capacitors voltage. In this modulation, the inner switches (e.g. S3 and S4 in Figure 1) operate at fundamental frequency and are switched based on the half-cycles of the reference waveform. The blocking voltage of these switches is twice the voltage of the outer switches.

4. Control Scheme of CS-DSTATCOM

The overall control scheme of the proposed CS-DTATCOM is illustrated in Figure 2. The overall control scheme consists of two main parts, i.e., internal control system and capacitors voltage balancing scheme.

- A DSTATCOM exchanges reactive power with the grid based on the grid requirements which is imposed by the grid operator. Also, an appropriate amount of real power has to be absorbed from the grid into the converter to keep the dc capacitors voltages charged. This is accomplished through the internal control system.
- Using the internal control system, the total real power which is needed to keep the average voltages of capacitors in the rated value is provided. Since, in CS-DSTATCOM, several dc voltage sources are replaced by dc capacitors, the absorbed real power should be distributed among the CS cells in such a way that each capacitor voltage to be balanced and regulated in the reference value. This aim is achieved by capacitor voltage balancing scheme.

The operation of internal control system is explained later in this section and the proposed capacitor voltage balancing scheme is illustrated in section IV.
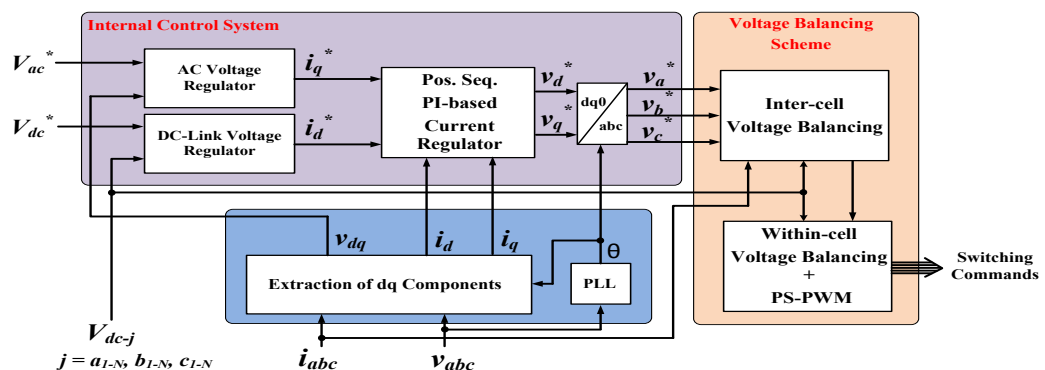

Figure 2. Overall control scheme of the CS-DSTATCOM

A. Extraction of dq components

The fundamental frequency components of the DSTATCOM voltage and current could be extracted using various techniques [25]. In the control system of the proposed CS-DSTATCOM, the three-phase time domain quantities are transformed to the rotational d-q reference fame. Accordingly, the control system of CS-DSTATCOM is designed based on PI controllers. Regarding Figure 3, at the first stage, the CS-DSTATCOM ac side voltage and currents and also dc side voltages are passed through a second-order low pass filter. This filter allows input signals to pass with frequencies less than the filter cut-off frequency with a specific damping factor and eliminate high frequency contents of the signals.

After filtering the CS-DSTATCOM voltage and current, they are initially converted into two-phase components in α-β frame by Clark transformation. Clark's transformation relationship is given as follows:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{1}$$

Then, the two-phase components in α-β frame are converted by park transformation into two-phase components in the d-q frame which is depicted in (2).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{2}$$
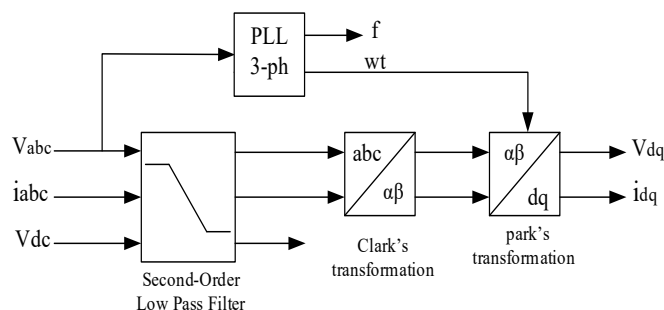
Figure 3. Block diagram for extracting d-q components of the voltage and current

Using (1) and (2), the converter ac side voltage is synchronized with the grid voltage. Note that, in (2), θ is the grid voltage phase angle which is obtained by a SRF phase-locked loop (PLL) [26]. In the same way, the CS-DSTATCOM output current is converted from three-phase quantities to two-phase quantities in d-q frame.

As shown in Figure 4, the main parts of internal control system include three regulator blocks, i.e., line voltage regulator, DC-link voltage regulator and current regulator block which are further explained in the following.

B. AC voltage regulator

The block diagram of the AC voltage regulator is shown in Figure 4. In this block, the amplitude of the grid voltage at the PCC, $|V_{dq}|$ obtained from (3) is compared with the reference value, $|V_{ac}|$. The resulting error produces the q-axis current reference, $i_{q\text{-ref}}$, through a PI controller. It is worth noting that in the case of grid voltage sag, the DSTATCOM acts in capacitive operation mode and the reactive current reference, $i_{q\text{-ref}}$, is increased to compensate under voltage in PCC. On the contrary, in over voltage condition, the DSTATCOM works in inductive mode and $i_{q\text{-ref}}$ is decreased to compensate voltage swell.

$$\left| V_{dq} \right| = \sqrt{V_d^2 + V_q^2} \tag{3}$$

C. DC-link voltage regulator

An ideal DSTATCOM does not consume active power because the output current and voltage are in quadrature. Hence, in multilevel DSTATCOMs, the dc power sources are replaced by dc capacitors. In CS-DSTATCOM, the mean value of the DC voltages in each basic unit does not change under ideal condition. In practice, to compensate the converter power loss and keep the dc capacitors voltages charged, a small amount of active power flows into the converter [27]. Accordingly, the dc capacitors voltages are regulated by controlling the active power flow into the converter which is done in DC-link voltage regulator. In this block, the reference dc voltage ($V_{dc\text{-ref}}$) is compared with the mean value of measured capacitors

voltage (V_{dc}). The resulting error generates the d-axis current reference, $i_{d\text{-}ref}$, through a PI controller. Note the $i_{d\text{-}ref}$ represents active current of CS-DSTATCOM and the mean value of all capacitors voltages in the whole converter is determined by controlling $i_{d\text{-}ref}$.
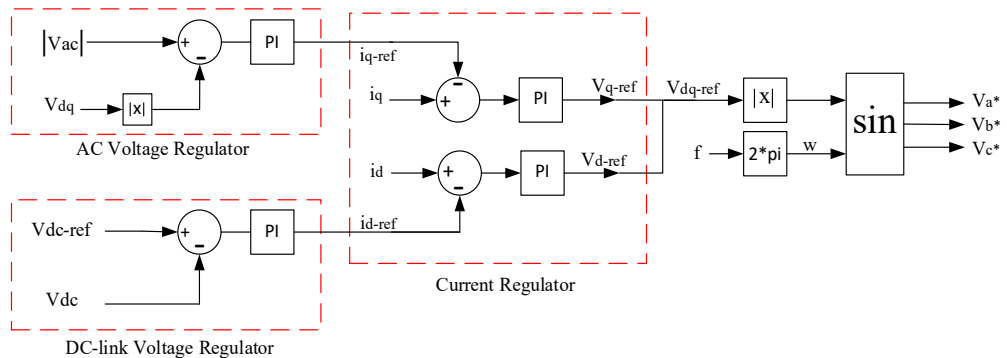

Figure 4. Block diagram of the internal control system, including AC voltage, DC-link voltage and current regulators

D. Current regulator

The current regulator block is located after two blocks of AC voltage regulator and DC-link voltage regulator. In fact, this block uses the outputs of the two previous blocks. As shown in Figure 4, the dq current components (i_{dq}), extracted from the DSTATCOM current, is given to the PI controllers along with the corresponding reference currents ($i_{dq\text{-}ref}$). In this block, each PI controller produces the reference voltage associated with the corresponding components.
Finally, the magnitude of the reference voltage, $V_{dq\text{-}ref}$, is given to the three-phase sinusoidal wave generator block. This block takes the reference voltage magnitude and the grid voltage phase angle and then produces a symmetric three-phase sinusoidal waveform. The resulting three-phase waveform is given to the voltage balancing scheme so that the switching signals are generated.
The DSTATCOM regulate the grid voltage at the PCC by injection or absorption of the reactive power. When the grid encounters an over-voltage, the DSTATCOM must absorb reactive power from the grid in order to reduce the PCC voltage. This work is done by injecting the inductive current into the grid, which means that the DSTATCOM acts in the inductive mode and the current is lag with respect to the PCC voltage. On the contrary, when the grid encounters under-voltage, the DSTATCOM enters the capacitive mode. In this case, the DSTATCOM current leads the PCC voltage and the reactive power is injected into the grid to regulate the PCC voltage.

5. DC-Link Capacitors Voltage Balancing

Using the internal control system, the desired reactive power is exchanged with the grid. Also, an appropriate amount of active power is absorbed to the converter to compensate the internal power loss. In a CS-DSTATCOM, each cell consists of two dc capacitor and also, several cells are connected in series in each converter leg. Hence, the absorbed active power into the CS converter has to be effectively distributed among the capacitors in such a way that each capacitor voltage to be kept in the reference value.
If the value of the capacitors of one basic unit is different from the others, the voltage of the capacitors of that unit will be different with those of other units. The unbalanced capacitors voltage causes to an increase in the total harmonic distortion (THD) [28] and may lead to capacitors voltage divergence and the converter interrupt. The dc voltage balancing is performed in two control levels, i.e., inter-cell and within-cell balancing which are discussed in sections V.A and V.B, respectively.

A. Inter-cell voltage balancing scheme

The working principle of the inter-cell voltage balancing is illustrated in Figure 5(a) and Figure 5(b) for capacitive and inductive operation modes, respectively.

a. Capacitive operation mode
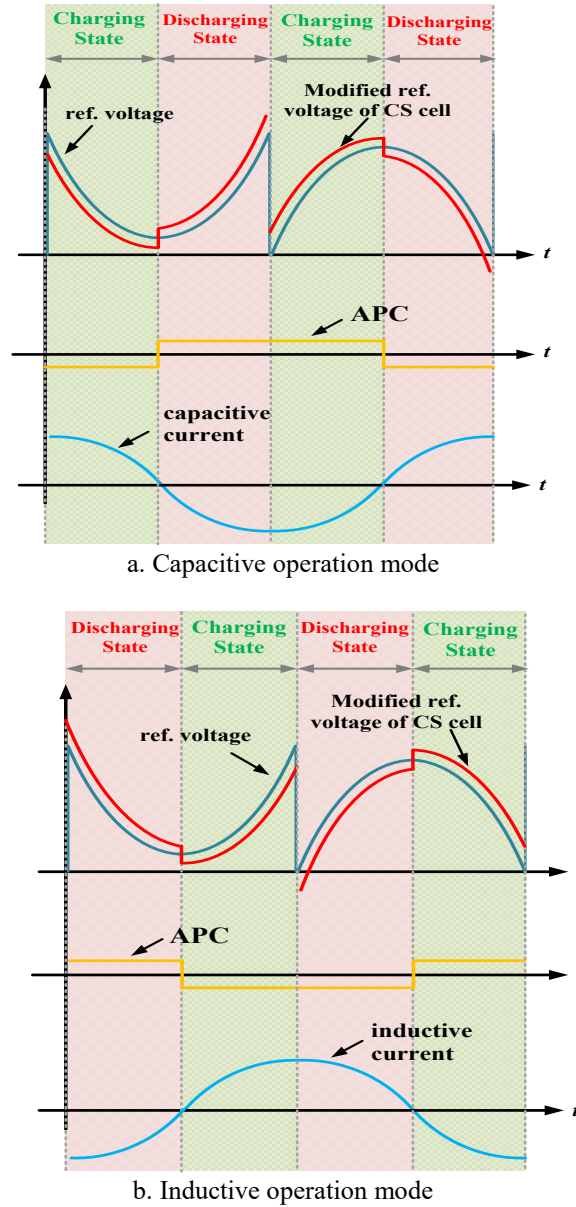

b. Inductive operation mode

Figure 5. Operation mechanism of the inter-cell voltage balancing scheme

As seen in Figure 5, an appendant component (APC) is added to the reference voltage of each cell. The magnitude of the APC depends on the cell average dc voltage and the phase of APC depends on the operation mode of CS-DSTATCOM. From Figure 5, it can be understood that the APC is added to the reference voltage of the cells in such a way that the cell with lower average dc voltage is charged and the cell with higher average dc voltage is discharged. The block diagram of the inter-cell balancing scheme is shown in Figure 6. In this block diagram, the APC magnitude is generated by PI controllers due to the deviation of cell average dc voltage from the reference value.
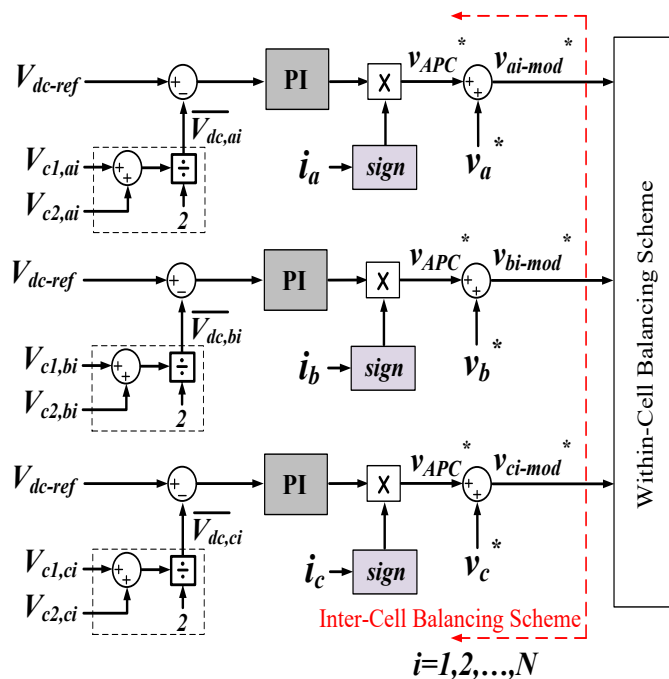
Figure 6. Block diagram of the inter-cell voltage balancing scheme

B. Within-cell voltage balancing scheme

Employing the inter-cell balancing system, average dc voltage of each cell is regulated at the reference value. However, each CS cell consists of two dc capacitors. Hence, another control system is needed to balance the voltage of capacitors within a cell. This aim is realized by within-cell balancing scheme which is depicted in Figure 7. As shown in the block diagram of Figure 7, the carriers that are used for outer switches in each basic unit are given phase shift. The value of the phase shift applied on the carriers is determined based on the voltage difference between the respective capacitor voltage and the average dc voltage of the cell. This action causes the energy of the capacitors to change. Using the PI controller, the amount of the carrier phase shift is controlled so that the voltage of capacitors within a cell to be equal with each other. The control system of Figure 7 is applied for each basic unit.
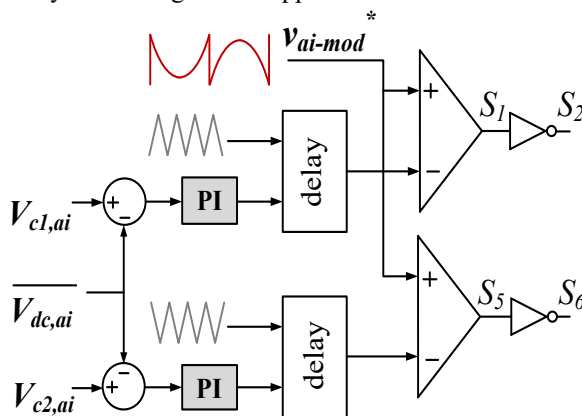

Figure 7. Block diagram of the within-cell voltage balancing scheme based on phase delay in the PS-PWM.

6. Design of a 11kV DSTATCOM

The CS-DSTATCOM consists of cascaded basic units, DC capacitors, AC inductors and a control system. The control system of the proposed CS-DSTATCOM was discussed in Section IV and V, and the design procedure of the other parts of the power circuit is presented as follows.

A. Number of basic units

In a CS-DSTATCOM, the number of basic units is one of the most important design parameters which also affects the blocking voltage of the power switches [29]. The desired CS-DSTATCOM is connected to a 11kV grid where the voltage magnitude of each phase ($V_{ph,m}$) is calculated based on (4).

$$V_{ph,m} = \sqrt{2}\, V_{LL} / \sqrt{3} \tag{4}$$

Due to (4), $V_{ph,m}$ is obtained 8.98kV. Table I indicates the relationship between the number of basic units and the rating voltage of the inner switches (the higher-voltage switches). If the number of basic units is considered to be 2, the rated voltage of the inner switches will be too high and the available commercial IGBTs are not able to withstand this voltage. If the number of basic units is considered to be 4, the rated voltage of the inner switches will be suitable, but the number of switches and capacitors is considerably increased which leads to a higher volume and cost. As a result, for the designed system, 3 basic units are selected by which the rating voltage of the switches is reduced to a level that the commercially available IGBTs can tolerate.

Table 1. The relationship between the number of basic units and Rating voltage of switches

Number of basic units	V_{switch}
2	4.5 kV
3	3 kV
4	2.25 kV

B. DC Capacitors (V_{dc} & C_{dc})

In the DSTATCOM structure, usually, all DC sources are replaced by capacitors, which makes the DSTATCOM to be able to exchange reactive power while the system cost and size is considerably decreased due to elimination of dc power sources. The capacitors voltage is determined based on the grid voltage. Also, the DC-link voltage should be kept at its minimum value to prevent the overvoltage on the switches and current distortion [30]. The minimum DC-link voltage for a DSTATCOM should be selected in a way that the maximum attainable output voltage of the DSTATCOM to be more than the grid voltage. Hence, the following equation is obtained:

$$\frac{\sqrt{3}M\,V_{dc}}{\sqrt{2}} \geq V_{LL} \tag{5}$$

Considering $M=1$, (4) results in:

$$V_{dc} \geq \frac{\sqrt{2}\,V_{LL}}{\sqrt{3}} \tag{6}$$

In (5) and (6), V_{dc} is the total DC-link voltage and M is the modulation index. Thus, for V_{LL} of 11kV, the minimum V_{dc} is obtained as 8.98kV and approximated as 9kV. In the CS-DSTATCOM, the DC-link includes six capacitors in each phase. Therefore, the minimum voltage of each capacitor is obtained as 1.48kV and is selected as 1.5 kV. There are two methods of calculating the capacitance of the DC-link capacitors; one method is based on the energy stored in the capacitors and desired hold up time and the other method (which is more

common) is based on the twice the grid frequency ripple of the capacitors voltage. These two methods are applied in the proposed CS-DSTATCOM capacitors design as follows:

B.1. Design of the Capacitors Based on the Stored Energy

In this methods, the capacitance of DC-link depends on the instantaneous energy available for the DSTATCOM during transient conditions [31]. According to principle of energy conservation and considering that each phase of CS-DSTATCOM consists of 6 capacitors, the capacitance of each capacitor is calculated according to the following equation.

$$6 \times \frac{1}{2} C \left[\left(V_{dc-ref} \right)^2 - \left(V_{dc-\min} \right)^2 \right] = V_{ph} (I_{ph}.a)t \tag{7}$$

Where, C is each capacitor size. In (7), V_{dc-ref} is the DC voltage reference, V_{dc_min} is the minimum voltage of each capacitor, a is the overloading factor, V_{ph} is the phase voltage, I_{ph} is the phase current, and t is the time by which the DC-link voltage is to be recovered. Considering V_{dc-min}=1.45kV, V_{dc-ref}=1.5kV, a=1.2, I_{ph}=120A, V_{ph}=9kV, t=300μs, C is obtained as 880uF.

B.2. Design of the Capacitors Based on the DC-Link Voltage Ripple

In this method, the double frequency voltage ripple of the DC-link capacitors is used for the size determination of them. In the DSTATCOM structures in which the DC-link of the three phases is not common, the dominant current flowing through the DC-link capacitors has a frequency twice of that of the output current. Also, the magnitude of the DC-link current dominant component will be equal to the magnitude of fundamental component of the output current. For example, if the output current frequency is 60Hz, the frequency of the dominant component of the DC-link current will be 120Hz. The double frequency voltage ripple of each DC-link capacitor in the proposed CS-DSTATCOM can be written as follows:

$$\Delta V_{cap,\max} = \frac{I_m}{2\omega C} \tag{8}$$

Where, I_m is the maximum magnitude of the fundamental component of the output current, $\Delta V_{cap,\max}$ is the maximum allowable double frequency voltage ripple on each DC-link capacitors and ω is the fundamental angular frequency.

For the designed case study with the rated reactive power of Q_{rated}, the following equation can be written:

$$Q_{rated} = 3 \times \frac{1}{2} V_m I_m \tag{9}$$

Using (9) and considering $Q_{rated} = 2MVAr$ and $V_m = 9kV$, I_m is obtained almost equal to 150A. If the maximum allowable voltage ripple on the capacitors is considered to be 10%, i.e. $\Delta V_{cap,\max} = 0.1 \times 1500V = 150V$, the minimum capacitance of each DC-link capacitors is obtained as follows using (8):

$$C = \frac{150}{2 \times 120\pi \times 150} = 1326\mu F \tag{10}$$

Considering the two methods of DC capacitors design, in the designed case study the value of each capacitor should be considered to be higher than 1326uF. In order to ensure that the capacitors will perform within the designed restrictions and also considering the tolerance of the capacitances in practice, the value of 1500uF is recommended for each capacitor.

Practically the DC electrolytic capacitors are used in the DC link. In order to reduce the negative effect of this type of capacitors equivalent series resistance (ESR) and also to better placement of the capacitors in the power circuit, several lower voltage and lower capacitance capacitors are used in series and parallel to fulfill the capacitance and voltage requirements.

C. Power switches

The main core of the CS-DSTATCOM is the CS voltage source converter, which includes fast switching semiconductor devices, such as IGBTs, MOSFETs and etc. The voltage ratings of the switches are determined based on the capacitors voltage of the DC-link and also their rating current depends on the required reactive power compensation, harmonic currents, and unbalance loading [32]. As the voltage of each capacitor is considered to be 1.5kV, the commercial IGBTs of voltage rating of 2.5kV are used for outer switches. Since the inner switches should tolerate twice the capacitors voltage (3kV), the commercial IGBTs of 4.5kV rating can be used for the inner switches. Also, as calculated before, the maximum magnitude of the output current is 150A. considering a safety factor, the power electronic switches with the rated continuous current of at least 200A is recommended.

D. AC Inductors (L_{AC})

The inductors are placed between the DSTATCOM and grid to filter high frequency components of the current [25]. The equation governing for the CS-DSTATCOM power circuit can be written as follows.

$$v_g + L_{AC} \frac{di}{dt} + Ri = v_{inv} \tag{11}$$

Where v_g is the instantaneous voltage at the PCC and v_{inv} is the output voltage of the inverter. When v_g is passing through the peak value (i.e. $v_g = V_m$) and during a switching interval of the CS-DSTATCOM power circuit, it can be assumed that v_{inv} is very close to the supply voltage [33]. The filter resistance is very small and can be ignored. So, equation (11) can be rewritten as follows:

$$L_{AC} = \frac{(v_{inv} - v_g)}{\frac{\Delta i}{\Delta t}} = \frac{\Delta v \times \Delta t}{\Delta i} \tag{12}$$

During a switching period, the inductor current increases when the inverter output voltage is higher than the grid voltage and it decreases when the inverter output voltage is lower than the grid voltage. Based on (12), the maximum inductance (design criterion) is obtained for maximum Δt and Δv, and minimum Δi. However, the maximum Δv occurs when Δt is minimum and vice versa. The worst case happens when $\Delta v = \frac{V_{step}}{2}$ and $\Delta t = \frac{T_S}{2}$, where, V_{step} is the voltage step of the inverter output voltage (1500V for the design case) and T_S is the effective switching period. It is important to note that as the interleaved PWM method has been used for modulation, the effective switching period is lower than the carrier waveforms period. The carrier signal frequency is f_c=1.5kHz, however, because of using interleaved PWM the effective switching frequency of the inverter output voltage is f_s=6×1.5kHz=9kHz. Therefore, the effective switching period is (1/9000)s, T_S=111us. Also, the maximum current ripple is considered to be 10% of the rated current peak value ($\Delta i = 0.1 \times 120\sqrt{2} \cong 17A$). Using these values and (12), L_{AC} is obtained as 2.5mH, which is considered 3mH per phase.

Finally, the switching frequency of the switches in the CS-DSTATCOM should be selected in a way that the highest order current harmonics be attenuated effectively.

The classification of the DSTATCOM topologies for the three-phase three-wire and three-phase four-wire distribution systems has been discussed in [32] where DSTATCOMs can be transformerless or with a transformer. The proposed CS-DSTATCOM is transformerless three-phase three-wire system and its design parameters for the 11kV distribution grid are given in the Appendix.

7. Simulation Results
A. Case Study and Simulation Parameters

The simulation has been carried out in Matlab/Simulink environment. The case study system is shown in Figure 8. As shown in the figure, the system includes a three-phase 11kV source with the Thevenin impedance denoted by Z_S. The source is followed by a 20km distribution feeder. At the end of the feeder, the proposed transformerless 13-level CS-DSTATCOM (as shown in Figure 1) is connected to the distribution grid. The feeder also feeds local loads via a step-down 11kV to 0.6kV transformer. The loads include constant and variable loads. The variable load is used to realize voltage variation in the system. In order to control the CS-DSTATCOM, the control system shown in Figure 2 is implemented in the Simulink. Parameters of the distribution system and the CS-DSTATCOM are shown in Table II, which are obtained based on the equations given in section VI. The rest of the parameters can be found in the Appendix.

Table 2. Circuit parameters of the case study

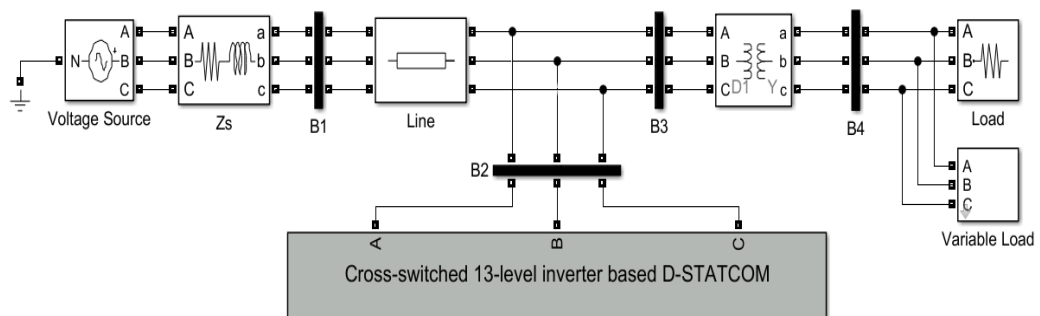| Parameter	Symbol	Value
Line to line rms voltage	V_{LL}	11kv
DC capacitor voltage	V_{dc}	1.5kV
Rated Capacity	Q_{rated}	2 MVAr
Carrier frequency	f_s	1.5kHz
Line frequency	f_c	60Hz
DC capacitor	C	1500uF
AC inductor	L_{AC}	3mH
Constant Load Power	P_L	1MW
Line length	L	20km
Source impedance	Z_S	$(0.121+j1.21)\Omega$

Figure 8. MATLAB-based model of the CS-DSTATCOM connected to a radial distribution system

B. Results and Discussion

The PCC voltage in normal condition is 1pu. In this condition, the DSTATCOM current is zero because there is no need for reactive power compensation. When an under/over voltage occurs at the PCC, the CS-DSTATCOM inject/absorb reactive power to keep the PCC voltage at the nominal value. As depicted in Figure 9, in the case study, first, the voltage reaches 1.1pu at t=0.15s, and then decreases to 0.9pu at t=0.3s.
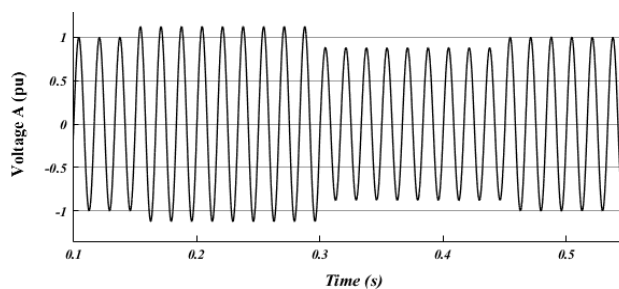
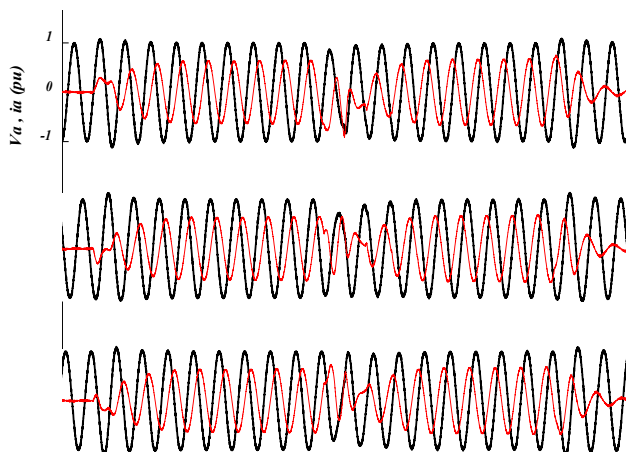Figure 9. PCC voltage without using CS-DSTATCOM

Figure 10. Three-phase CS-DSTATCOM currents and PCC voltage.

The PCC voltage and the CS-DSTATCOM current are shown in Figure 10. First, the line voltage is equal to the nominal value, and the injected current into the grid is zero. At t=0.15s, the line voltage increases to 1.1 pu and the CS-DSTATCOM enters the inductive mode and the current lags the grid voltage. At t=0.3s, the line voltage decreases to 0.9 pu, and the CS-DSTATCOM acts in capacitive mode and the current leads the grid voltage. The variation amount of the grid voltage determines the amplitude of the injected current. Finally, at t=0.45s, the line voltage returns to its nominal value, so the injected current decreases to zero.

The output voltage of the CS converter for a basic unit and a cluster is shown in Figure 11. It is observed that the basic unit voltage is a 5-level waveform with the amplitude of 3kV, and the cluster voltage is a 13-level waveform with the amplitude of 9kV. At t=0.3s the output voltage changes because of the change in the operation mode of the CS-DSTATCOM. Figure 11 shows that the capacitors voltage is maintained at the rated value during the dynamic condition which proves the proper operation of the internal control system.

Table 3 shows the THD values of the injected current, the converter output voltage, and the PCC voltage for phase A in both inductive and capacitive operation modes. It can be seen that the THD of the current in both cases is less than 2% and the CS-DSTATCOM injects a high-quality current to the grid which is in accordance with IEEE 519.

Figure 12 shows the PCC voltage with and without using CS-DSTATCOM. Regarding this figure, the proposed CS-DSTATCOM properly responds to the grid voltage fluctuations and regulates PCC voltage to the nominal value of 1pu.
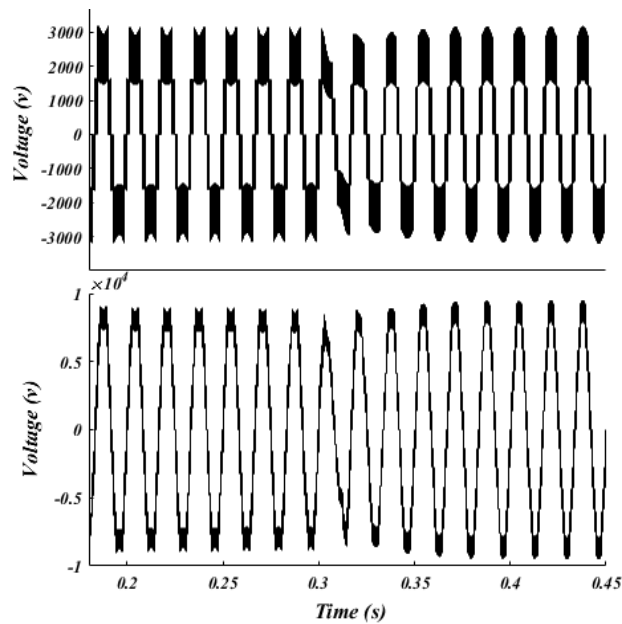
Figure 11. The output voltage of the basic unit and a cluster in CS-STATCOM.

Table 3. THD values of PCC voltage, convertre output voltage and injected current

		Parameter		
		PCC voltage	Converter output voltage	Injected current
Mode	Inductive (t<0.3s)	2.33	10.12	1.80
	Capacitive (t>0.3s)	2.24	9.46	1.73

Figure 13 shows the active and reactive power of the CS-DSTATCOM. As seen in this figure, the active power absorbed to the CS-DSTATCOM is negligible in steady state condition. When the PCC voltage is 1pu, the exchanged reactive power is also zero (no current is injected to the grid). Regarding Figure 13, at t=0.15s when the grid voltage increases, the DSTATCOM operates in inductive mode and absorbs reactive power from the grid to compensate the over voltage. At t=0.3s, when the grid voltage decreases, the DSTATCOM operation mode is changed to capacitive mode to inject the reactive power to the grid and increase the PCC voltage. The magnitude of exchanged reactive power in both operation modes is 2MVAr.
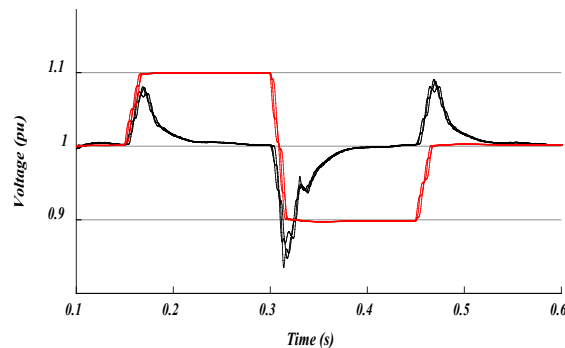

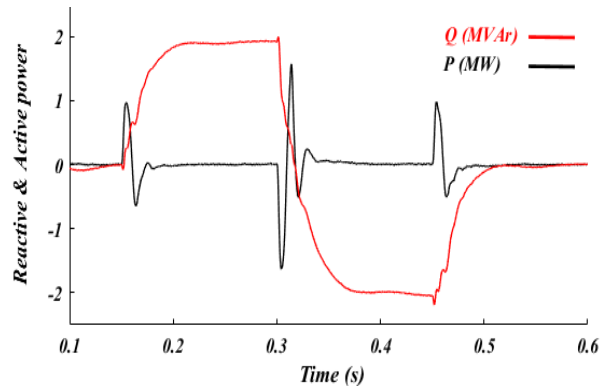Figure 12. The PCC voltage with and without utilizing CS-DSTATCOM.

Figure 13. The exchanged active and reactive power between the CS-DSTATCOM and the grid.

Figure 14 shows capacitors voltage in the case that all dc link capacitors are the same capacity. The voltage of three capacitors in different phases are demonstrated in Figure 14. According to this figure, the capacitors voltage is well adjusted in the rated value with a ripple of less than 10%. It is seen that the control system keeps the capacitors voltage balanced during the dynamic condition when the CS-DSTATCOM operation mode is changed from inductive to capacitive mode.
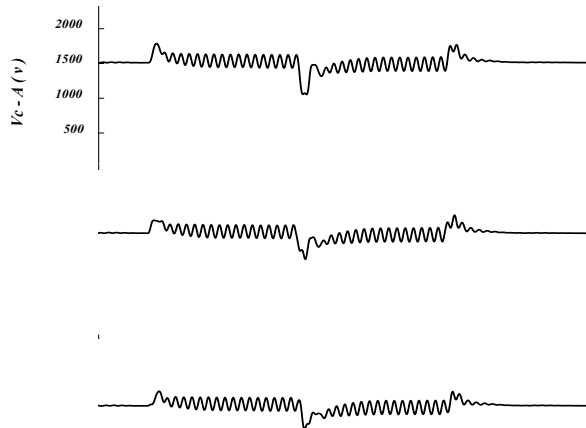

Figure 14. Capacitors voltage in the case of using same capacitance in three clusters.

In order to study the performance of the presented capacitor voltage balancing scheme, the capacitance of the two capacitors in a basic unit of a cluster is set to be different from the nominal value of 1 mF. The capacitance of one of them is considered to be 10% higher and that of the other to be 10% lower than the nominal value. Hence, the voltage of the capacitor with more capacitance, decreases; and voltage of the capacitor with lower capacitance, increases. However, by applying the proposed voltage balancing scheme, the capacitors voltages are balanced regardless of different values of their capacitances. Figure 15 shows the voltage of three capacitors; one of them with the nominal capacitance (V_{cn}) and the two others with 10% higher and 10% lower capacitances (V_{c1} and V_{c2}). As the figure indicates, all capacitors voltage

is kept at the rated value of 1.5 kV validating the performance of the proposed balancing scheme.
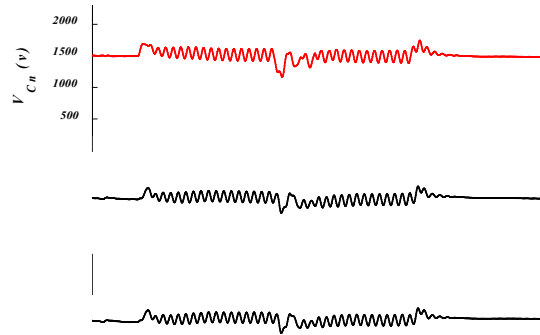

Figure 15. Capacitors voltage in the case of different capacitance (Vcn: nominal, Vc1:10% higher, and Vc2:10% lower than rated value).

The overall comparison of the proposed CS-DSTATCOM and the other multilevel inverter based DSTATCOM structures is presented in Table IV for a 13-level output voltage case study. It is important to note that as the number of voltage levels is kept constant for all of the structures, their performance in terms of the output voltage and current harmonics is almost identical. The comparison includes the number of power components and performance indexes. As the table indicates, in the proposed 13-level CS-DSTATCOM, 6 capacitors and 18 power electronic switches are utilized per phase, while the in CHB-DSTATCOM, 6 capacitors and 24 power electronic switches are used for the same number of voltage levels. Other multilevel inverter based DSTATCOMs such as the neutral-point-clamped (NPC) multilevel inverter based DSTATCOM (NPC-DSTATCOM), the flying-capacitor (FC) multilevel inverter based DSTATCOM (FC-DSTATCOM), and the modular multilevel converter (MMC) based DSTATCOM (MMC-DSTATCOM) use considerably more power electronic switches. Moreover, the proposed uses the least number of capacitors and it does not require clamping diodes. Considering the table, the proposed CS-DSTATCOM and the CHB-DSTATCOM have identical specifications whereas the CHB-DSTATCOM uses more power electronic switches.

Table 4. Comparison of DSTATCOM based on different MLI topologies

		CS-DSTATCOM	CHB-DSTATCOM	NPC-DSTATCOM	FC-DSTATCOM	MMC-DSTATCOM
Number of Power Components per phase (13-level)	Power switches	18	24	24	24	48
	Capacitors	6	6	12	13	24
	Clamping diodes	-	-	22	-	-
Performance in DSTATCOM application	Modularity	YES	YES	NO	YES	YES
	Voltage balancing capability	High	High	Low	Low	High
	Maximum feasible voltage levels	No limitation	No limitation	5	7	No limitation
	Complexity of Control System	Low	Low	Medium	Medium	High

8. Conclusion

In this paper, a transformer-less DSTATCOM based on cross-switched (CS) multilevel inverter has been presented and its configuration, capacitor voltage balancing scheme and design procedure have been studied. Modularity is one of the advantages of the CS inverter which can be easily extended to higher voltage levels and be directly connected to distribution grid without the need for bulky and heavy transformers. The cascaded configuration of the CS cells reduced the output voltage harmonics and caused to the removal of passive shunt filters. The CS inverter generates the same voltage level using fewer number of power components in comparison with CHB inverter, making the CS an ideal candidate for DSTATCOM application. Each CS cell consists of two capacitors and several capacitors are used in each converter phase. Hence, a hierarchical scheme has been proposed for capacitors voltage balancing for CS-DSTATCOM consisting of inter-cell and within-cell balancing schemes. In the inter-cell balancing system, the average dc voltage of CS cells is balanced and regulated in the rated value, while in within-cell balancing scheme, the capacitors voltages within a cell are balanced. The proposed control system performed the balancing of the capacitors voltage in both the same and different capacitances conditions. Several simulation results have been carried out in MATLAB/SIMULINK environment validating the performance of the proposed CS-DSTATCOM for grid voltage regulation at a 11 kV distribution system. As the results indicated, the proposed STATCOM operated successfully in bus voltage regulation in both capacitive and inductive mode. According to the results, it is able to compensate for ±10% bus voltage variation with response time of less than 50ms. Also, the output waveform quality is high so that the THD of the injected current is lower than 1.8%.

APPENDIX
Line to line voltage: V_{LL} = 11kV
Grid frequency: f_s = 60Hz
Number of basic units: n = 3
Maximum modulation index: M= 1
DC-link voltage in each phase: $V_{dc\text{-}ph}$ = 9kV
Number of capacitors per phase = 6
Minimum DC voltage of capacitor: $V_{dc\text{-}min}$ = 1.45kV
DC voltage of each capacitor: V_c = 1.5kV
Reference DC voltage of capacitor: $V_{dc\text{-}ref}$ = 1.5kV
Capacitance of DC capacitors: C = 1500uF
AC inductor: L_{AC} = 3mH
PS-PWM switching frequency: f_c = 1.5kHz
IGBT for outer switches: 2.5kV, 200A, 0.78kW
IGBT for inner switches: 4.5kV, 200A, 1.44kW
Rated reactive power: Q = 2MVar
Line length: L = 20km
Transformer: three-phase Δ/Y transformer with the rating of 11kV/0.6kV, 6MVA
Variable load: V_n = 0.6kV, I_n = 3kA, pf = 0.9

9. References

[1]. P. Kumar and Informatics, "Comparative Power Quality analysis of Conventional and Modified DSTATCOM Topology," *International Journal on Electrical Engineering and Informatics*, vol. 9, no. 4, pp. 786-799, 2017.
[2]. Y. Koyama, Y. Nakazawa, H. Mochikawa, A. Kuzumaki, K. Sano, and N. Okada, "A Transformerless 6.6-kV STATCOM Based on a Hybrid Cascade Multilevel Converter Using SiC Devices," *IEEE Transactions on Power Electronics,* vol. 33, no. 9, pp. 7411-7423, 2018.

[3]. R. Sajadi, H. Iman-Eini, M. K. Bakhshizadeh, Y. Neyshabouri, and S. Farhangi, "Selective Harmonic Elimination Technique With Control of Capacitive DC-Link Voltages in an Asymmetric Cascaded H-Bridge Inverter for STATCOM Application," *IEEE Transactions on Industrial Electronics,* vol. 65, no. 11, pp. 8788-8796, 2018.

[4]. Y. Neyshabouri and H. Iman-Eini, "A New Fault-Tolerant Strategy for a Cascaded H-Bridge Based STATCOM," *IEEE Transactions on Industrial Electronics,* vol. 65, no. 8, pp. 6436-6445, 2018.

[5]. Y. Neyshabouri, S. K. Chaudhary, R. Teodorescu, R. Sajadi, and H. Iman-Eini, "Improving the Reactive Current Compensation Capability of Cascaded H-Bridge Based STATCOM under Unbalanced Grid Voltage," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* pp. 1-1, 2019.

[6]. J. Jung, J. Lee, S. Sul, G. T. Son, and Y. Chung, "DC Capacitor Voltage Balancing Control for Delta-Connected Cascaded H-Bridge STATCOM Considering Unbalanced Grid and Load Conditions," *IEEE Transactions on Power Electronics,* vol. 33, no. 6, pp. 4726-4735, 2018.

[7]. X. Liu, J. Lv, C. Gao, Z. Chen, and S. Chen, "A Novel STATCOM Based on Diode-Clamped Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* vol. 32, no. 8, pp. 5964-5977, 2017.

[8]. G. Farivar, C. D. Townsend, B. Hredzak, J. Pou, and V. G. Agelidis, "Low-Capacitance Cascaded H-Bridge Multilevel StatCom," *IEEE Transactions on Power Electronics,* vol. 32, no. 3, pp. 1744-1754, 2017.

[9]. E. Kontos, G. Tsolaridis, R. Teodorescu, and P. Bauer, "High Order Voltage and Current Harmonic Mitigation Using the Modular Multilevel Converter STATCOM," *IEEE Access,* vol. 5, pp. 16684-16692, 2017.

[10]. H. Chen and P. Cheng, "A DC Bus Voltage Balancing Technique for the Cascaded H-Bridge STATCOM With Improved Reliability Under Grid Faults," *IEEE Transactions on Industry Applications,* vol. 53, no. 2, pp. 1263-1270, 2017.

[11]. P. Wu, H. Chen, Y. Chang, and P. Cheng, "Delta-Connected Cascaded H-Bridge Converter Application in Unbalanced Load Compensation," *IEEE Transactions on Industry Applications,* vol. 53, no. 2, pp. 1254-1262, 2017.

[12]. E. Behrouzian, M. Bongiorno, and R. Teodorescu, "Impact of Switching Harmonics on Capacitor Cells Balancing in Phase-Shifted PWM-Based Cascaded H-Bridge STATCOM," *IEEE Transactions on Power Electronics,* vol. 32, no. 1, pp. 815-824, 2017.

[13]. M. M. Bhesaniya and A. Shukla, "Current Source Modular Multilevel Converter: Detailed Analysis and STATCOM Application," *IEEE Transactions on Power Delivery,* vol. 31, no. 1, pp. 323-333, 2016.

[14]. G. Farivar, B. Hredzak, and V. G. Agelidis, "Decoupled Control System for Cascaded H-Bridge Multilevel Converter Based STATCOM," *IEEE Transactions on Industrial Electronics,* vol. 63, no. 1, pp. 322-331, 2016.

[15]. Y. Shi, B. Liu, Y. Shi, and S. Duan, "Individual Phase Current Control Based on Optimal Zero-Sequence Current Separation for a Star-Connected Cascade STATCOM Under Unbalanced Conditions," *IEEE Transactions on Power Electronics,* vol. 31, no. 3, pp. 2099-2110, 2016.

[16]. H. Chen, P. Wu, C. Lee, C. Wang, C. Yang, and P. Cheng, "A Flexible DC Voltage Balancing Control Based on the Power Flow Management for Star-Connected Cascaded H-Bridge Converter," *IEEE Transactions on Industry Applications,* vol. 52, no. 6, pp. 4946-4954, 2016.

[17]. H. Chen, P. Wu, C. Lee, C. Wang, C. Yang, and P. Cheng, "Zero-Sequence Voltage Injection for DC Capacitor Voltage Balancing Control of the Star-Connected Cascaded H-Bridge PWM Converter Under Unbalanced Grid," *IEEE Transactions on Industry Applications,* vol. 51, no. 6, pp. 4584-4594, 2015.

[18]. R. Xu *et al.*, "A Novel Control Method for Transformerless H-Bridge Cascaded STATCOM With Star Configuration," *IEEE Transactions on Power Electronics,* vol. 30, no. 3, pp. 1189-1202, 2015.

[19]. Y. Neyshabouri, H. Iman-Eini, and M. Miranbeigi, "State feedback control strategy and voltage balancing scheme for a transformer-less STATic synchronous COMpensator based on cascaded H-bridge converter," *IET Power Electronics,* vol. 8, no. 6, pp. 906-917, 2015.

[20]. Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM With DC-Link Capacitor Voltage Balancing Control for Diode-Clamped Multilevel Converter Based STATCOM," *IEEE Transactions on Industrial Electronics,* vol. 60, no. 5, pp. 1884-1896, 2013.

[21]. M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE transactions on power electronics,* vol. 28, no. 2, pp. 625-636, 2013.

[22]. E. Babaei, M. F. Kangarlu, M. Sabahi, and M. R. A. Pahlavani, "Cascaded multilevel inverter using sub-multilevel cells," *Electric Power Systems Research,* vol. 96, pp. 101-110, 2013.

[23]. M. F. Kangarlu and E. Babaei, "Cross-switched multilevel inverter: an innovative topology," *IET Power Electronics,* vol. 6, no. 4, pp. 642-651, 2013.

[24]. M. F. Kangarlu, E. Babaei, and M. Sabahi, "Cascaded cross-switched multilevel inverter in symmetric and asymmetric conditions," *IET Power Electronics,* vol. 6, no. 6, pp. 1041-1050, 2013.

[25]. B. Singh and J. Solanki, "A comparison of control algorithms for DSTATCOM," *IEEE transactions on Industrial Electronics,* vol. 56, no. 7, pp. 2738-2745, 2009.

[26]. G.-C. Hsieh and J. C. Hung, "Phase-locked loop techniques. A survey," *IEEE Transactions on industrial electronics,* vol. 43, no. 6, pp. 609-615, 1996.

[27]. K. Sano and M. Takasaki, "A transformerless D-STATCOM based on a multivoltage cascade converter requiring no DC sources," *IEEE transactions on power electronics,* vol. 27, no. 6, pp. 2783-2795, 2012.

[28]. J. A. Barrena, L. Marroyo, M. Á. R. Vidal, and J. R. T. Apraiz, "Individual voltage balancing strategy for PWM cascaded H-bridge converter-based STATCOM," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 1, pp. 21-29, 2008.

[29]. H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," *IEEE Transactions on Industry Applications,* vol. 43, no. 4, pp. 1041-1049, 2007.

[30]. H. Akagi, E. H. Watanabe, and M. Aredes, *Instantaneous power theory and applications to power conditioning*. John Wiley & Sons, 2017.

[31]. B. Singh, P. Jayaprakash, and D. Kothari, "A T-connected transformer and three-leg VSC based DSTATCOM for power quality improvement," *IEEE Transactions on Power Electronics,* vol. 23, no. 6, pp. 2710-2718, 2008.

[32]. B. Singh, P. Jayaprakash, D. P. Kothari, A. Chandra, and K. Al Haddad, "Comprehensive study of DSTATCOM configurations," *IEEE Transactions on Industrial Informatics,* vol. 10, no. 2, pp. 854-870, 2014.

[33]. B. Singh, P. Rastgoufard, B. Singh, A. Chandra, and K. Al-Haddad, "Design, simulation and implementation of three-pole/four-pole topologies for active filters," *IEEE Proceedings-Electric Power Applications,* vol. 151, no. 4, pp. 467-476, 2004.

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